A highly integrated GaAs MMIC UHF band demodulator with four tunable quadrature phase shift IF channels

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***Abstract* – A MMIC demodulator has been designed and characterized over the [0.79 – 0.97] GHz RF band. It consists of an RF differential amplifier and an LO 4-way phase splitter affording the 0°, 90°, 180° and 270° relative phase shift and equal amplitude signals. Both RF and LO channels drive a double double balanced quad FET mixer which provides the four quadrature phase shift voltage baseband IF signals on high outputs impedances.**

This chip (4 x 3.1 mm²) has been fabricated using a GaAs 0.5µm MESFET process and reaches a high performance as far as IF signals balance accuracy is pursued.

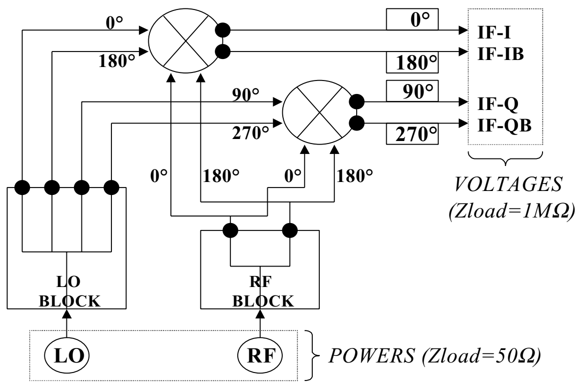

Fig. 1. Block diagram of the demodulator

I. INTRODUCTION

In miscellaneous RF applications such as cellular phones or space satellites, the improvement in semiconductor technology, with a higher integration level of RF/IF and digital functions, leads to the choice of a direct « RF to IQ baseband » conversion for new receivers architectures.

In this paper, we present a highly-integrated demodulator chip, allowing an electronic adjustement of the IF outputs relative phase shifts. With a –6 dBm LO drive, the chip is designed for the [0.79 – 0.97] GHz RF band and can provide four quadrature phase shift IF baseband voltage signals on identical 1 MΩ loads. The 3 dB IF bandwidth is [0 – 100] MHz.

II. TOPOLOGY

The configuration of the demodulator is shown in Figure 1. The mixing cells structure is a quad of four cold MESFETs whose gates are driven by the LO signal. This topology was selected to comply with the linearity specification.

The LO splitter (figure 2.) providing the 0°, 90°, 180° and 270° relative phase shift signals is made with a second order all-pass RC network [1], followed by five differential stages to insure the right phase imbalance as well as the required signal level to drive the mixing cells. In spite of more voltage losses, the RC topology allows a higher integration level compared to inductors network in the UHF band.

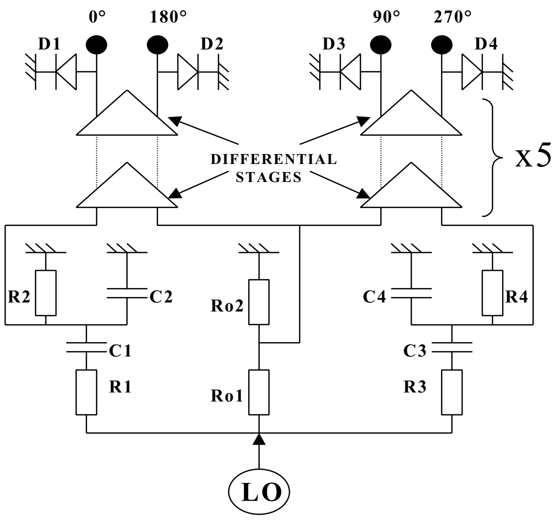

Fig. 2. LO block topology

One FET diode (1µm gate length) per LO channel has been added to adjust the shift imbalance if necessary. The tuning window (several degrees) is enough to compensate for the spread process as well as the variations versus frequency.

The RF splitter is made with an active balun [2] followed by a self biased differential stage (figure 3.), which includes an active load bias network [3] in addition. This topology (figure 4.) is reported to be less sensitive to bias variations. Moreover, it provides a solution to avoid inductors bias network, hence a more effective integration on the chip.

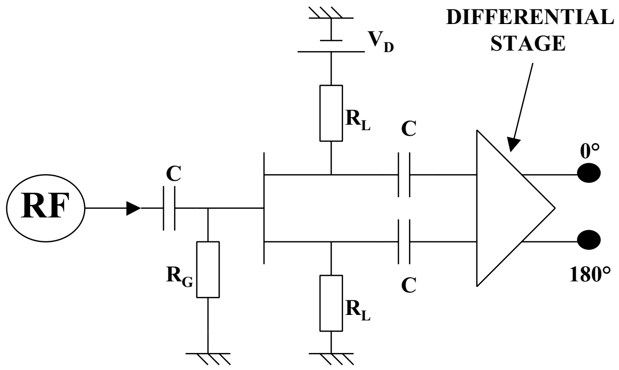

Fig. 3. RF block topology with an active balun

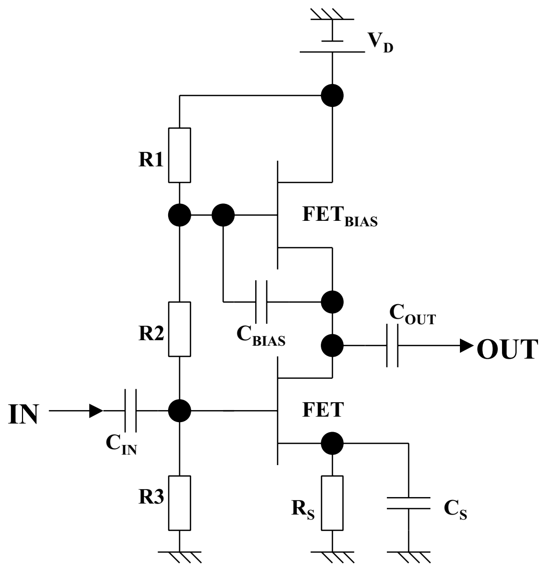

Fig. 4. Active load & self bias topology

III. FABRICATION AND TEST

Figure 5 shows the 4 x 3.1 mm² chip, based on a GaAs 0.5µm MESFET process which is less susceptible to ionic radiations than Si process, for space applications. The test bench especially requires a 12 DC probe card, as well as four identical low-pass filters in order to reject the image-frequency part of the quadrature phase shift IF signals. The outputs voltage measurement will simultaneously be achieved by a four channels oscilloscope (internal impedance : 1 MΩ)

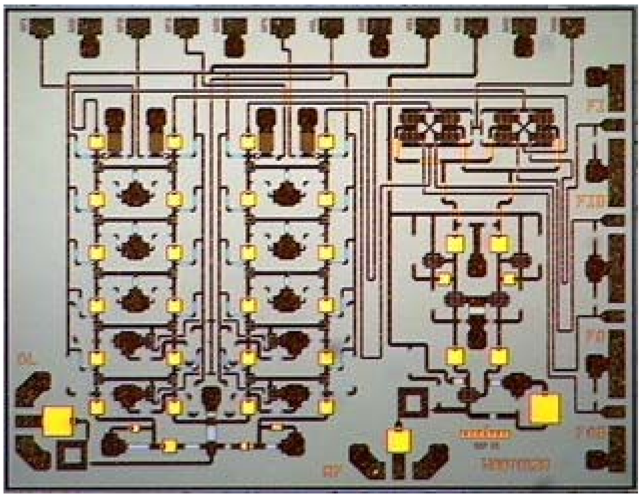

Fig. 5. Photograph of the demodulator MMIC

IV. PERFORMANCES

The chip DC consumption is less than 780 mW under 5 Volts. RF frequency is set to 860 MHz while IF frequency will be fixed to 1 MHz for the all next tests. Bias voltages {VP1,…VP4} driving the LO channel diodes will all be set to an average value of –1 Volt. The RF input one dB compression point is up to +2 dBm. Figure 6 simultaneously shows the four IF voltage signal waveforms for an RF input power of –10 dBm.

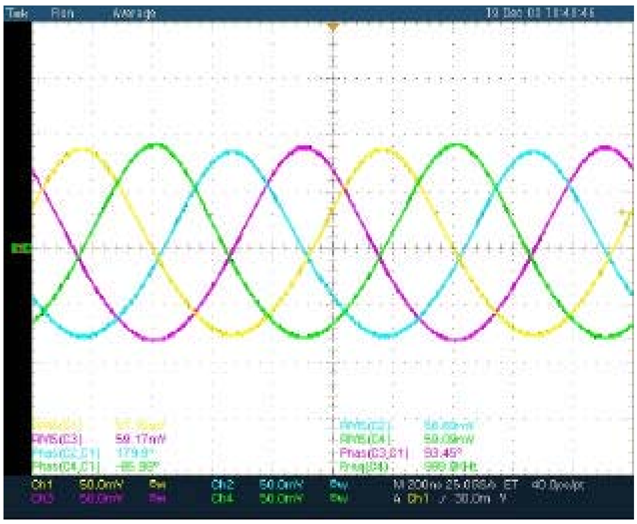

Fig. 6. IF voltage waveforms versus time

Figure 7 shows the IF signals voltage level versus RF frequency. Figure 8 and 9 respectively show the IF signals amplitude and phase imbalance errors (better than 0.5 dB and 5° respectively).

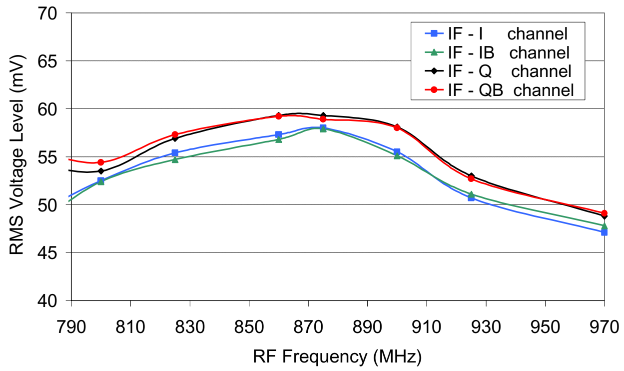

Fig. 7. RMS Voltage Level versus RF Frequency

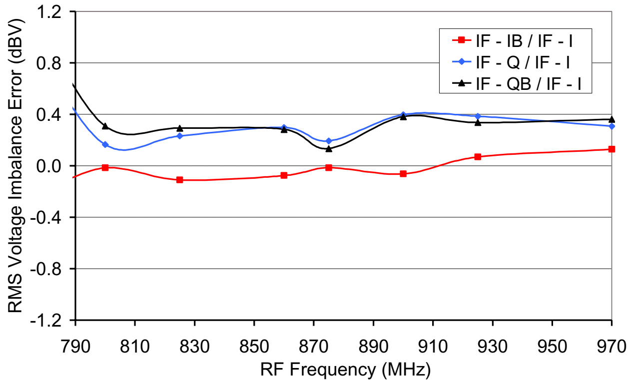

Fig. 8. RMS Voltage Imbalance Error versus RF Frequency

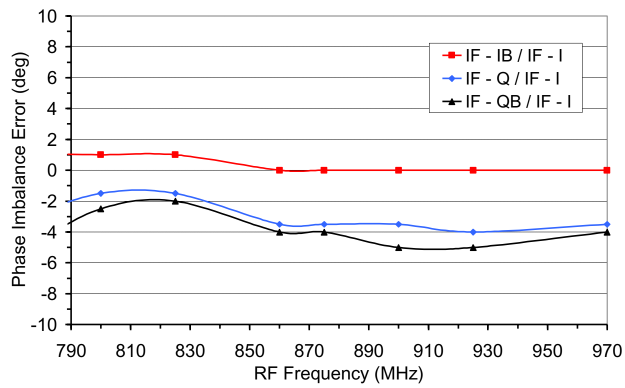

Fig. 9. Phase Imbalance Error versus RF Frequency

Figure 10 shows the corrective effect of the four diodes driven by {VP1,...,VP4} voltages in the window : [-2 ; 0] V. After tuning, this test has shown a relative phase imbalance error better than 0.5° between all four quadrature IF signals, with a minor impact on the amplitude imbalance (less than 0.1 dB).

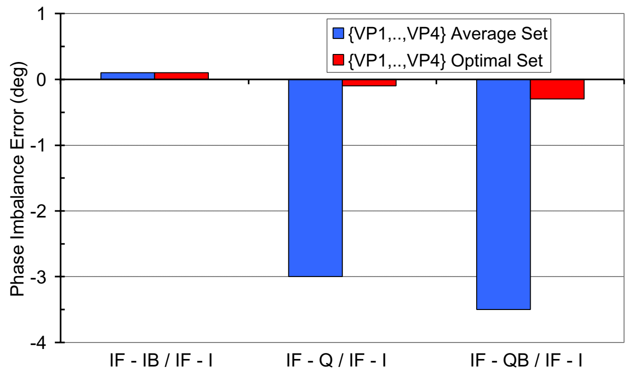

Fig. 10. Phase Imbalance Error Tuning
@ RF Frequency = 860 MHz

V. CONCLUSION

A MMIC UHF demodulator has been designed and tested on a GaAs 0.5µm MESFET process. This chip can cope with high integration requirements (chip size : 4 x 3.1 mm²), linearity and signal balance high performances (0.6dB & 0.5° after tuning), especially thanks to its phase shift tuning availability. With a direct RF to baseband down-conversion, this topology may bring a positive answer to new receiver equipments specifications.

REFERENCES

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