Coplanar W-Band Low Noise Amplifier MMIC Using 100-nm Gate-length GaAs PHEMTs

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***Abstract* — This paper presents the performance of a W-band low noise amplifier MMIC, based on coplanar technology, and utilizing 100-nm gate-length GaAs pseudomorphic power HEMTs. With a chip size of less than 2 mm^2, this two-stage LNA achieves a small signal gain of more than 12 dB between 90 and 100 GHz, with 12.5-dB gain and 3.9-dB noise figure at 94 GHz. This is the best reported performance for power PHEMT-based LNAs at W-band, which is also comparable to the best results reported with more advanced InP or Metamorphic HEMT low noise technologies.**

I. Introduction

Passive and active imaging systems in the millimeter-wave range have created a demand for low-noise amplifier (LNA) MMICs with high gain, large bandwidth and low power consumption. Thus, to address these applications, Indium Phosphide (InP), and other related metamorphic HEMTs, have been the subject of constant development over the last ten years, due to their excellent transport properties [1-4]. However these technologies still suffer from higher manufacturing cost, lower breakdown voltage, and device reliability issues compared to conventional GaAs PHEMTs.

In this paper, we report the performance of a coplanar two-stage 94-GHz LNA MMIC, using pseudomorphic GaAs HEMTs. Compared to InP or MHEMT [5], the maturity of GaAs PHEMT technology is more advanced, offering more robust devices, and higher power densities at higher breakdown voltage. Already widely in production, this technology takes the advantage of a rapidly growing wafer size, up to 6 inches today, at the lower cost. Moreover, 100-nm gate length devices provide significant improved gain and noise performance compared to existing 0.15-µm GaAs PHEMTs, without a sharp technology shift. Besides, the coplanar waveguide (CPW) technology is very attractive at millimeter wave frequencies due to: the simplified fabrication process, excluding the necessity of backside metallization and via-hole processing, the higher isolation between adjacent lines, and its compatibility with flip-chip packaging, among other advantages [1,2,6].

II. MMIC Technology

The W-band LNA MMIC was fabricated on several pseudomorphic 4''-GaAs wafers. Based on the UMS 0.15-µm power PHEMT technology, the structure of the double-side doped epitaxy was scaled down for the use of 100-nm class T-gates (22% InGaAs PHEMT), as shown in Fig. 1. This millimeter-wave power process features typically an extrinsic transit frequency f_T of more than 150 GHz at 3-V drain bias, a peak transconductance g_{max}=750 mS/mm, a maximum drain current density $J_{d,max}$ of 650 mA/mm, and more than 7-V gate-drain breakdown voltage. Due to short source-drain spacing, the source and drain resistances are as low as $R_s < 0.4\ \Omega{\cdot}$mm. All coplanar MMICs are realized on 635-µm thick substrates, with two gold metallization levels, 30 Ω/□ TaN resistors, 250 pF/mm^2 SiN MIM capacitors, and airbridge technology.

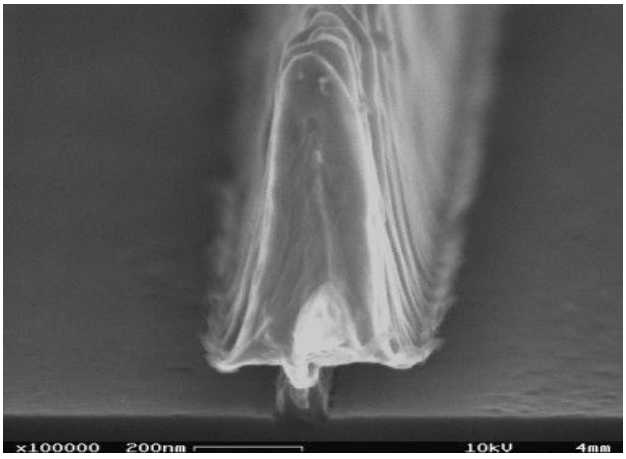

Fig. 1: SEM microphotograph of UMS 100-nm gate length GaAs PHEMT technology.

III. MMIC Design

A photograph of the W-band MMIC amplifier is shown in Fig. 2. The two-stage amplifier consists of 2×20 µm PHEMT devices having source inductive lines, for simultaneous gain and noise matching. The LNA MMIC size is less than 2.0×1.0 mm^2. Further size reduction, up to 0.5 mm^2, is possible, by removing the 50-Ω line at the output side.

A rigorous methodology was used for the design of the coplanar MMIC low noise amplifier. Optimum source match, and power transfer were considered in the optimization of gain, bandwidth, and noise figure. In order to achieve compact size, the bias networks were directly integrated into the T-matching networks, and the interstage was optimized for direct impedance transformation. Circuit stability was also of primary

concern. Therefore, feedback source lines, large on-chip bypassing capacitors, and appropriate out-off band resistive loading were used to stabilize the LNA for the best trade-off between noise figure and gain, resulting in unconditional stability of the amplifier over the entire frequency range.

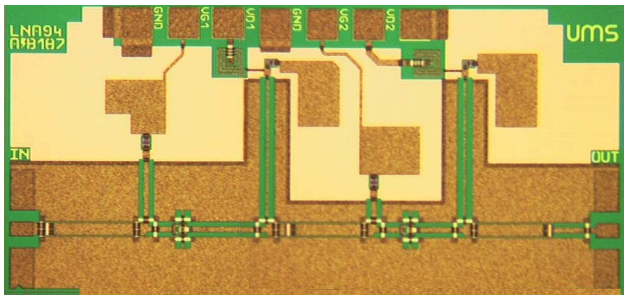

Fig. 2: Chip photograph of the W-band coplanar LNA (chip size is 2.0 × 1.0 mm^2).

A. PHEMT device optimization

From preliminary characterization level, it could be estimated, that the best compromise between noise figure and gain, is obtained while the PHEMT devices are operated at 250 mA/mm drain current, for a drain voltage of 1.5 V. Then, the single device gate width, and the number of gate fingers were optimized for minimum noise figure at the highest associated gain, on the basis of the scalable small signal equivalent circuit model represented in Fig. 3.

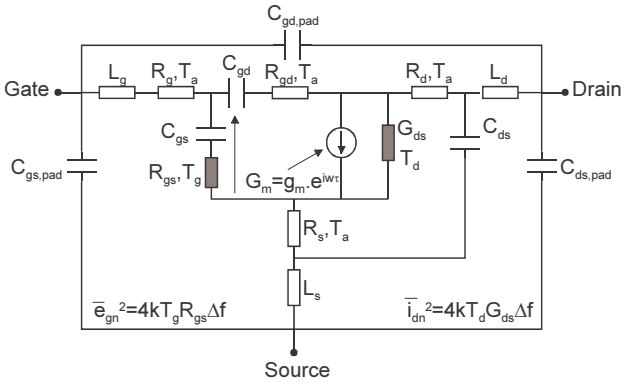

Fig. 3: Small signal equivalent FET & noise model used for the 100-nm GaAs PHEMT technology.

The noise figure optimization is performed by means of the Pospiezalski model [7]. This simple model, compatible with the above small signal equivalent circuit, enables to represent the noise dependence through only two parameters T_g and T_d, being the equivalent noise temperatures of the gate-source R_{gs} and drain-source R_{ds} resistances respectively. In the present case, all resistive elements have an equivalent noise temperature of T_a=298 K, except the channel resistance 1/G_{ds}, which has a higher equivalent noise temperature of T_d=2100 K at 250-mA/mm drain current. Fig. 4 shows the minimum noise figure NF_{min}, and the total input resistance $R_{tot} = R_g + R_{gs} + R_s$, as a function of the total gate width W_g. For the simple equivalent temperature model of [7], short gate widths give the lowest noise figure. However, our in-house noise model (dashed line), described with different formalism and other noise sources, shows an optimum plateau near the 40-µm gate width range. This behavior was traded off with the optimum gate width W_g for minimum input resistance, thus enabling higher gain per stage. The optimum gate width for minimum input resistance can be calculated from the small signal equivalent model of Fig. 3, and equals:

$$W_{g,\min} = \sqrt{\frac{r_s + r_{gs}}{r_g}}, \qquad (1)$$

leading to a minimum input resistance $R_{tot,min}$=10.3 Ω for a gate width of 70-µm. Nevertheless, as the 40-µm device gives a lower noise figure for a comparable input resistance (i.e. 12 Ω), a 2 × 20 µm PHEMT device was finally chosen. An additional motivation for choosing this device geometry was that this gate width, and number of gate fingers, were used for model extraction. Therefore, the small signal model is much more accurate than any other, scaled down from a different device geometry.

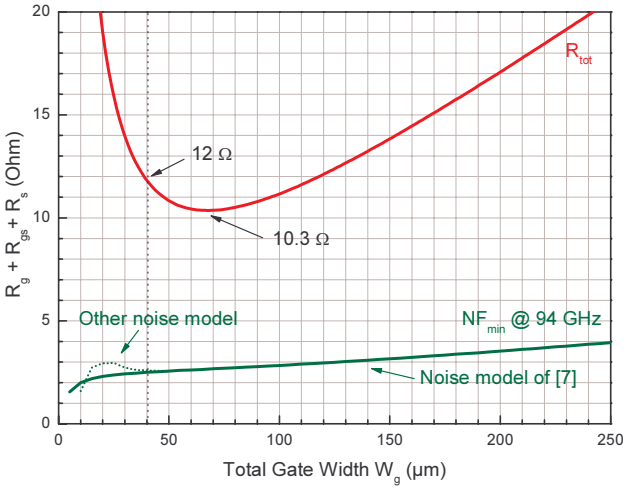

Fig. 4: Simulated total input resistance, and minimum noise figure (f=94 GHz) as a function of the gate width for a 2-finger 100-nm GaAs PHEMT (V_d=1.5 V, I_d=250 mA/mm).

B. Coplanar element models

Accurate passive element modeling is essential at W-band frequencies. The passive circuit simulation relies on an accurate coplanar element model library, derived from the characterization of experimental test structures, validated up to 120 GHz [6]. All CPW elements have a ground-to-ground spacing of 50 µm. Furthermore, line loss is considered in all coplanar devices.

An important coplanar element is the T-junction, which represents one of the most difficult discontinuities to model, because its electrical parameters depend strongly on the stub length, termination impedance, and become frequency dependent at millimeter-wave frequencies. A small error in the phase shift due to the branch line of the CPW T-junction, can lead to significant mismatch in the overall design at W-band. Precise models for the CPW T-junction (Fig. 5) use sections of transmission lines, and airbridges, with section parameters Z_c and ε_{re}, being extracted from measurements of various test structures. For model verification, test structures with cascaded elements in series (up to 8), were measured. The stubs

are terminated with a short, for compatibility with a two-port S-parameter measurement system. Fig. 6 shows a comparison between modeled, and measured S-parameters for eight coplanar T-junctions (30-Ω ports) connected in series. Excellent agreement was obtained in both magnitude, and phase up to 120 GHz [6].

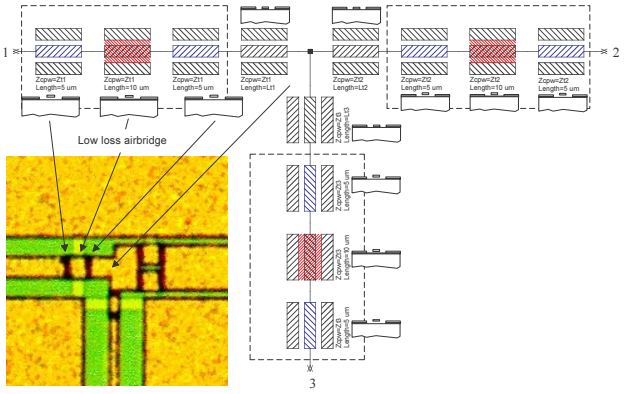

Fig. 5: Broadband transmission line based model for the coplanar T-junction (picture: 50/70/30-Ω junction).

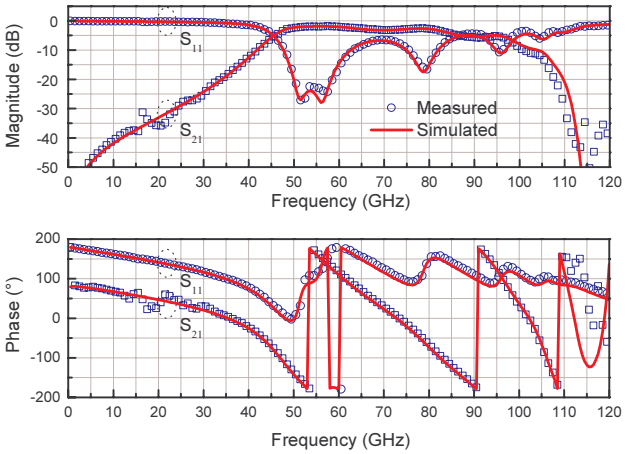

Fig. 6: Comparison between simulated- (solid curves), and measured (symbols) S-parameters of 8 cascaded coplanar 30-Ω T-junctions, over the 0.5-120 GHz frequency range.

III. Measured Performance

The S-parameters of the LNA MMICs were measured with an Anritsu® 0.5-110 GHz ME78O8A vector network analyzer. Fig. 7 shows typical on-wafer small signal S-parameters, and noise figure from 75 to 105 GHz. At a drain voltage of 1.5 V, and a total current of 20 mA (identical bias for each stage), this first-pass design LNA demonstrates more than 10-dB gain (S_{21}) from 80 to 100 GHz, and 12.5-dB gain at 94 GHz. Input- (S_{11}), and output- (S_{22}) return loss is above 20 dB at 94 GHz, which is very good for this frequency band. The reverse isolation (S_{12}) is better than 20 dB over the entire frequency range.

The device noise figure was characterized with the *FhG*-IAF noise measurement setup described in [8]. Using the same bias conditions, an average noise figure (NF) of 3.8 dB was measured between 90 and 100 GHz (Fig. 7, NF_{94GHz}=3.9 dB). Fig. 8, shows the measured noise figure and associated gain for different bias conditions. The best performance was achieved at V_d=1.5 V and 10-mA drain current, with an average noise figure of only 3.6 dB, and 10.3-dB associated gain across the same frequency band (NF_{94GHz} < 3.7 dB). Noise figures as low as 3.1 dB, with 10-dB associated gain were also measured at 99 GHz.

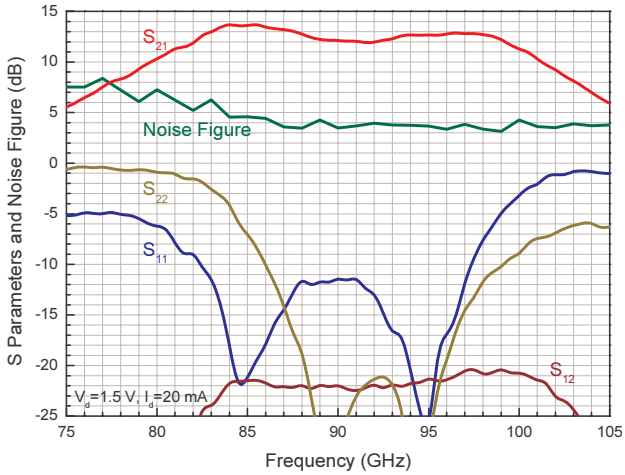

Fig. 7: On-wafer measured S-parameters and noise figure of the W-band LNA MMIC at V_d=1.5 V, and I_d=20 mA (75-105 GHz).

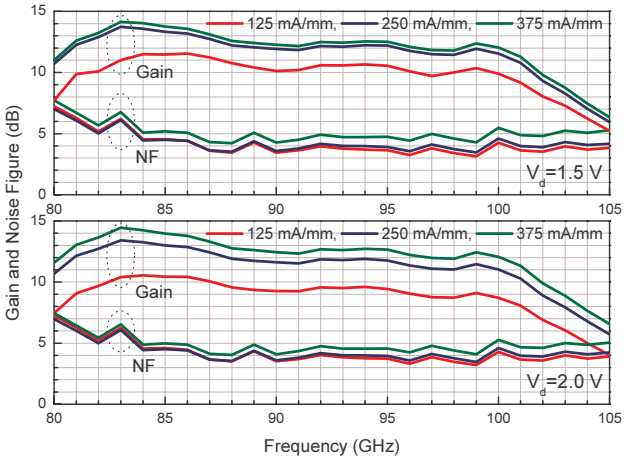

Fig. 8: Measured gain and noise figure of the W-band LNA at V_d=1.5 V (top), and V_d=2.0 V (bottom).

Finally, Table I summarizes the state-of-the-art for two-stage W-band LNA MMICs, realized in different technologies. The performance reported in this paper using 100-nm GaAs power PHEMTs, compares well to the best results achieved with noise-optimized InP HEMT- or MHEMT devices, respectively.

Table I: Comparison of various reported two-stage W-band LNA MMICs.

Freq. [GHz]	Gain [dB]	NF [dB]	Technology	Ref.
80-90	8.5	3.5	100-nm MHEMT	[2]
95	20	2.5	100-nm InP	[3]
89	14	4.8	100-nm MHEMT	[4]
94	30	4.0	100-nm GaAs Low Noise PHEMT	[9]
94	13	2.3	70-nm MHEMT	[1]
90-100	10.3 12.5	3.6 3.8	100-nm GaAs Power PHEMT	this work

IV. Conclusion

The performance of a W-band low noise amplifier MMIC, based on coplanar technology, and utilizing 100-nm gate-length GaAs pseudomorphic power HEMTs, has been presented. The device geometry and bias were optimized for best gain and noise figure. With a chip size of less than 2 mm^2, this two-stage LNA achieves a small signal gain of more than 12 dB between 90 and 100 GHz, with 12.5-dB gain, and 3.9-dB noise figure at 94 GHz, which is the best reported performance for power PHEMT-based LNAs at W-band, and is also favorably comparable to the best results reported with more advanced low noise InP or Metamorphic HEMT technologies.

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