Design Data for Hot-via Interconnects in Chip Scale Packaged MMICs up to 110 GHz

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***Abstract*— Theoretical and experimental design data for the modeling of bump- to hot-via interconnect transitions, for use in chip-scale package MMICs, is presented. The theoretical data is based on cascaded analytical transmission line models, derived from rigorous electromagnetic analysis. Excellent agreement has been observed between theory and experiment up to 110 GHz. This modeling approach is validated with the characterization of a broadband millimeter-wave PHEMT amplifier MMIC using the hot-via and bump interconnects, for mounting on a carrier substrate; the measurements are as well, in very good concordance with the predicted performance, including the effects of BCB coating, backside metallization and bump- to hot-via transitions.**

I. INTRODUCTION

The trend of monolithic microwave, and millimeter wave integrated circuits (MMIC) is toward cost effective packaged products, compatible with Surface Mount Device (SMD) assembly line [1]. Among the number of existing microwave packages (e.g. ceramic, flange mount, gull wing, micro-leadframe, etc.), one of the most promising solution, for next generation of wafer-level packaging technologies, is the Chip Scale Packaged (CSP) MMIC [2,3]. CSP refers to an encapsulated device whose the total volume is only 1.5 times bigger than the bare die MMIC, and that has RF and DC interconnects compatible with printed circuit board (PCB) line resolutions. CSP is cost effective since it is a collective wafer-level packaging process, that includes, in one step, both the package and IC assembly, without wire bonding. Whereas the flip-chip approach, in combination with coplanar MMICs, provides very good RF and thermal properties, up- and above the millimeter-wave range [4], most existing microwave ICs are still designed with the microstrip technology. In this frame, the hot-via concept represents a relevant alternative to flip-chip, especially for millimeter wave CSP MMICs. With hot-vias, the MMIC is mounted face-up, by mean of bumps connecting the backside to a carrier substrate, e.g. aluminum nitride (AlN), alumina (Al_2O_3), low temperature co-fired ceramic (LTCC), or even soft organic substrates like Rodgers RO4003. Fig. 1 illustrates one possible configuration of hot-via CSP MMIC: Coplanar transmission lines on carrier (Fig 1-a) connect the backside of the MMIC, using solder bumps (Fig. 1-b) to an RF pad (Fig. 1-c); this pad being connected to the front-side of the MMIC (Fig. 1-e,f) using standard via-hole technology (Fig. 1-d). Each of these elements represents a different section of transmission line, in which the RF signal is propagating. In addition to its inherent compatibility with microstrip MMICs (but not limited to), the hot-via mounting provides simultaneously reproducible electrical, thermal, and physical attachment of the MMIC to the "outer world", alleviating technical problems like bond wire parasitic inductance, additional mounting steps, chip alignment, etc. Furthermore, this technique can be used with surface mount assembly production lines, and the MMICs can be visually inspected after mounting [5].

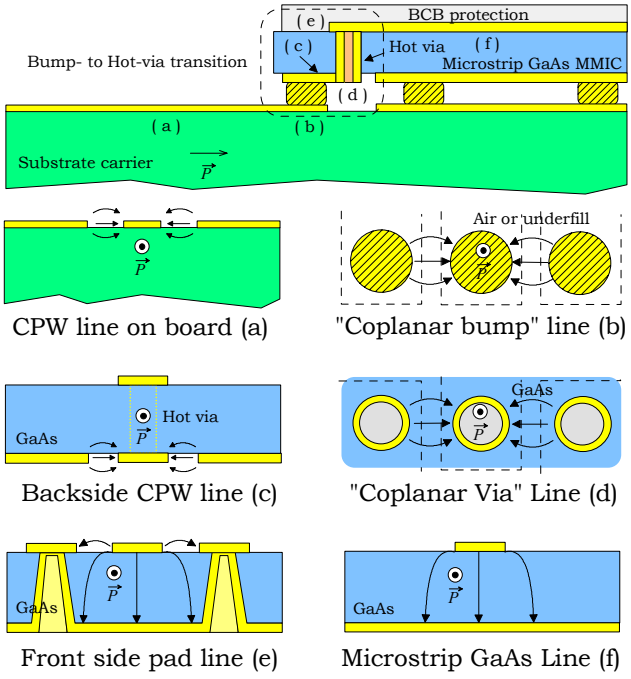

Fig. 1. Principle of "hot-via" CSP MMIC, mounted on a carrier plate with bumps, and different cross sections, with corresponding transmission lines. The Poynting vector *P* indicates the direction of the main quasi-TEM mode.

Relatively few work has been reported on hot-via technique, and relatively few design data exists [3,5]. Because there is a need for extremely broadband circuits in microwave and optoelectronic communication and radar systems, models which are applicable from DC over 100 GHz are required. Especially, scalable models are important considering different technologies. This paper presents such broadband models, validated with experimental design data, and performance for the bump-to-hot-via (BHV) interconnects, for use in chip scale packaged millimeter-wave ICs up- and above W-band.

II. Models for RF Bump- and Hot-Via Interconnects

The present work was realized with the UMS Pseudomorphic HEMT MMIC technology on 100-µm thick 4'' GaAs substrates, via-holes with 30-µm diameter, 75-µm diameter bumps and 25-µm height, the front-side being fully coated with a 7-µm thick BCB layer. Microphotographs illustrating key process features, are shown in Fig. 2. Different configurations of RF bumps-, and hot-via transitions were investigated, and optimized for broadband operation. In the proposed model, the transitions are represented with sections of quasi-TEM transmission lines, as shown in Fig. 1. The propagation characteristic parameters for each section (Fig. 1-b to f), such as the characteristic impedance Z_c, the effective relative dielectric constant ε_{re}, and the attenuation α, are obtained from rigorous 3D electromagnetic (EM) analysis, as well as analytical forms, resulting in models fully scalable with dimensions, and material properties.

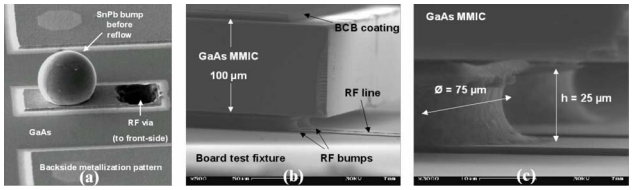

Fig. 2. Microphotographs of CSP MMICs using hot-vias, and bump attach on carrier substrate: a) backside RF pad before bump reflow soldering, b) die attach on carrier substrate, c) enlarged view of the bump transition.

A. "Coplanar bump-", and "hot-via" lines

Bumps in air, and hot-via lines in insulating gallium arsenide (GaAs, ε_r=12.9) were investigated. For the theoretical analysis, the commercial finite integration method in time domain of CST Microwave Studio® was used. The transition between the coplanar line on the carrier substrate (Fig. 1-a), and the backside of the chip, is realized with a "coplanar bump" line (Fig. 1-b). The transmission line parameters Z_c, ε_{re}, and α, are extracted for each frequency, from the S-parameters computed with the numerical EM simulations, by mean of the method described in [6]. As for Z_c, the imaginary part of the impedance is negligibly small at millimeter wave frequencies, its contribution has been neglected. Therefore, only the real part of the impedance, Re(Z_c), is presented.

One important design parameter for the bump line is its form factor, given by the bump diameter t and the ground-to-ground spacing D, as illustrated in Fig. 3 (medallion). In Fig. 3, the electro-magnetically computed characteristic impedance is presented as a function of the frequency, for different diameters t (symbols). It can be seen that at millimeter-wave frequency, Z_c can be considered as frequency independent, which holds for $\varepsilon_{re}\approx 1$, as well. Fig. 4 (symbols) also shows the extracted characteristic impedance, as a function of the ground- to ground spacing D, for different realistic bump diameters. For 75-µm bumps, the characteristic impedance ranges from 20- to 100 Ω. It is interesting to mention that 50-Ω is only achieved for values of D smaller than 200 µm. Practically, such dimensions can only be processed with high-density-resolution metal deposition. For lower resolution, as used with soft materials (e.g. PCB, organic substrates), larger values should be used, typically 300-µm or greater. Yet from Fig. 4, for 75-µm bumps and 300-µm ground- to-ground spacing, the characteristic impedance is 100 Ω. Although relatively high, this value is not a performance issue, since the bump height is often relatively small, i.e. only 25 µm. Meanwhile, other ways to lower Z_c, are to use either a dielectric underfill, or to increase the bump diameters. For the hot-via line, the characteristic impedance follows similar variations, as shown on Fig. 3- and 4; the characteristic impedance is however much lower for comparable dimensions, because of the higher dielectric loading from GaAs, compared to air. In this line configuration, the 50-Ω impedance is easily obtained with current MMIC process resolutions.

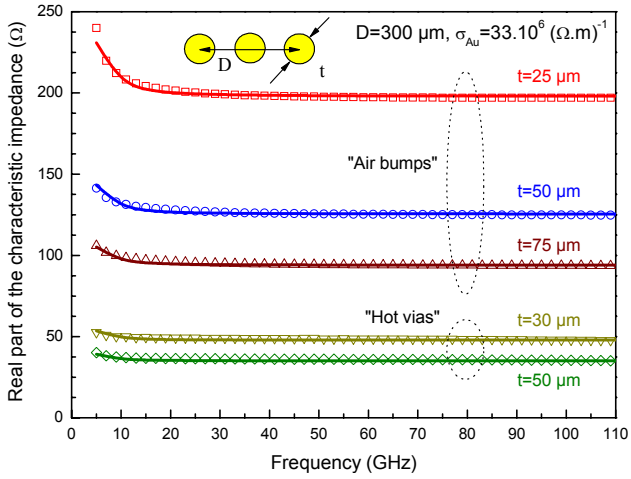

Fig. 3. Characteristic impedance of "air coplanar bumps", and "GaAs coplanar via", versus frequency, for different conductor diameters (symbols: EM, solid: analytical model).

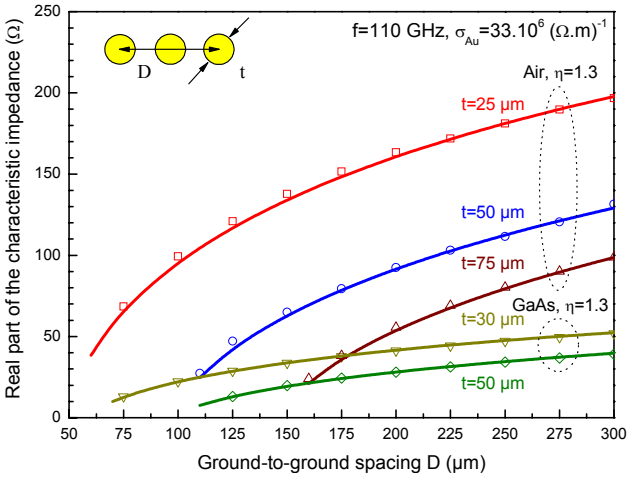

Fig. 4. Characteristic impedance of "air coplanar bumps", and "GaAs coplanar vias" line, for different diameters. (symbols: EM simulations, solid: analytical model).

B. Analytical models

Scalable analytical models are of great help when designing bump- to hot-via transitions. Therefore, in a second approach, the bump or hot-via lines are modeled with original closed-form approximations, derived from

that of the *two-parallel-wire* characteristic impedance, for which an exact analytical solution exists [7]. The advantage of such a formulation compared to pure fit power functions, is the better physical relevance. The modified characteristic impedance, developed for the coplanar bump- or hot-via lines, is given as:

$$Z_c = \frac{120}{\eta\sqrt{\epsilon_r}} \ln\left(\frac{D}{2t} + \frac{1}{2}\sqrt{\left(\frac{D}{2t}\right)^2 - 1}\right) \cdot M$$

where to a first order approximation, $\eta \approx 1.3$, and M is a frequency dependent parameter, approaching 1 at high frequencies. For the bump line, as a result of the homogeneous transmission line structure in air, $\varepsilon_{re}=1$. Figures 3-, and 4 show comparisons between the theoretical characteristic impedance (symbols), and the proposed analytical form (solid lines). A very good agreement is observed between both analysis for various dimensions of the coplanar bump line. Similarly to the "coplanar bump" line, the characteristic impedance of "coplanar via" lines is expressed with the same formula, except that as the line is embedded in homogenous GaAs, the effective relative dielectric constant becomes $\varepsilon_{re}=12.9$. From the results obtained in Fig. 3-, and 4, it can be assumed that this model is valid, at least within the range $2 \cdot t \le D \le 12 \cdot t$, and $1 \le \varepsilon_r \le 13.1$. Finally, in all methods, loss are considered, with a frequency dependent attenuation, fitted with a power function, in the form of $\alpha=\alpha_0 \times f^n$, n approaching ½ at high frequencies.

C. *Backside coplanar RF pad*

The backside contact pad (Fig. 1-c) which connects the bumps (Fig. 1-b) to the hot-vias (Fig. 1-d), and also serves as probing pad for on-wafer measurements, is a coplanar waveguide section (CPW). Thus, its propagation characteristics can be easily determined from the quasi-TEM descriptions available in the literature [8]. For this coplanar line section however, as a result of its relatively wide dimensions, the open-end effects occurring at both ends of the line, can not be neglected. The fringing fields can be modeled by a simple equivalent capacitance [9]. However, the simple design rules of [9] does not apply for such small gap width, and therefore a more accurate model for the equivalent fringing capacitance C_{open}, has been developed [10]. Fig. 5 shows the behavior of such open-end capacitance as a function of gap width g, for different line dimensions $k=w/d$. Very good model agreement is obtained for typical values extracted from measurements on gallium arsenide. As shown in Fig. 5, the capacitance can not be neglected at millimeter wave frequencies for large dimensions, as in the backside line.

Finally, the complete model for the bump- to hot- via transition, fully scalable with dimensions and material properties, is presented in Fig. 6. For the "coplanar bump" line section, the length is that of the bump height h, let $l_{BU}=25\mu m$; for the "coplanar via" line, the length is that of the substrate thickness, let $l_{hv}=100$ µm. The length of the coplanar RF pad section is 130 µm.

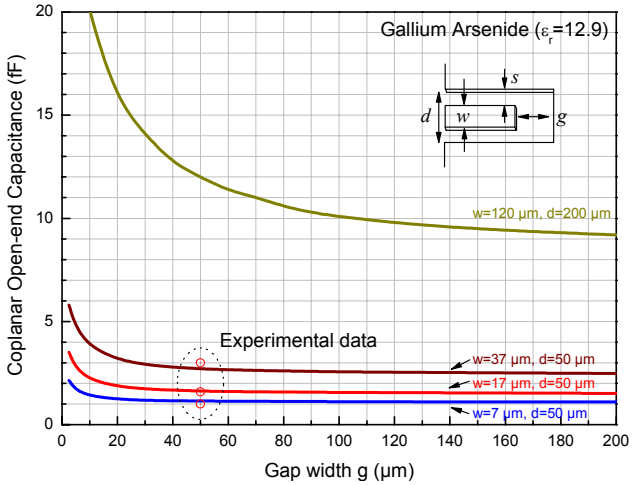

Fig. 5. Coplanar open-end capacitance model as a function of gap width, and line dimensions w, d (GaAs).

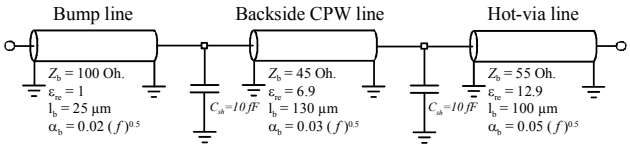

Fig. 6: Broadband transmission-line based model for the bump/hot-via transition as used in the test structure of Fig. 7.

III. EXPERIMENTAL RESULTS

A. *Bump- to hot-via transition test structure*

The proposed transition models were validated with the S-parameter measurements of appropriate test elements in the millimeter wave range. Fig. 7 shows an example of test structure, used for the characterization of one possible configuration of bump/hot-via interconnects. It consists of a 50-Ω coplanar line on a carrier substrate, connected with bumps, and hot-vias to a microstrip line on the GaAs test MMIC. The Fig. 8 presents a comparison between the simulation using the electrical models (solid lines), and the measured S-parameters (symbols) for the transmission line test structure of Fig. 7-a. The simulation of the whole structure, with the complete transition model, is in very good agreement with the measured S-parameters, in both magnitude and phase, i.e. within ±0.5 dB ∠ ±2 ° standard error deviation, up to at least 110 GHz. Yet on Fig. 8, are plotted the S-parameters extracted from a single bump- to hot-via transition (dashed lines). Very low insertion loss (S_{21}) over the frequency band, namely less than 0.6 dB per transition at 110 GHz, is achieved. The associated return loss is also reasonable, i.e. $|S_{11}|<-10$ dB at 110 GHz, and can be easily compensated with the on-chip matching networks during the MMIC design phase.

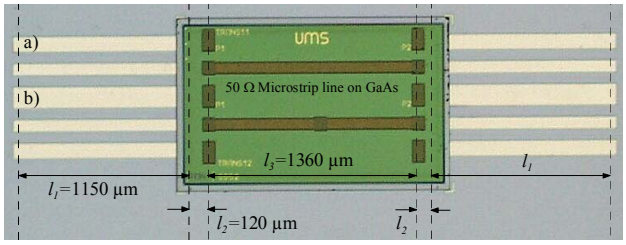

Fig. 7. Transmission line test structure used for bump- to hot-via characterization (a: thru-line, b: shorted line).

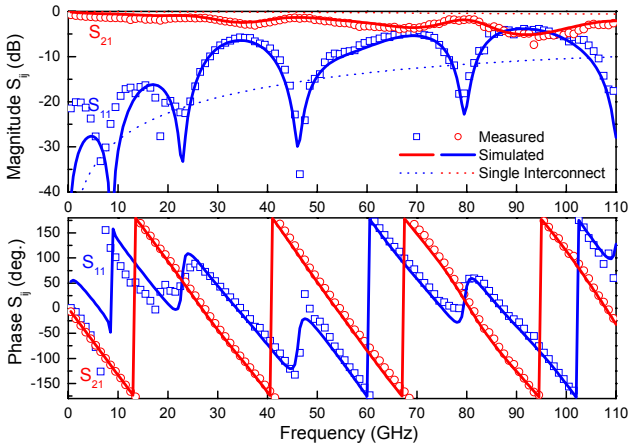

Fig. 8. Comparison between measured and simulated S-parameters of the thru-line test structure shown in Fig. 7-a.

To better fit the simulated S-parameters to those obtained from measurements, direct optimization of the different electrical parameters of the transition model, was also performed. Results from this parameter optimization, in comparison to those obtained from analytical forms, are summarized in Table I: a very good agreement for all parameters is obtained between theory and optimization, which demonstrates that the quasi-TEM transmission line approach is suitable for bump- to hot-via transition modeling, up to at least 110 GHz.

TABLE I: THEORY VERSUS BEST MEASUREMENT FIT

Electrical parameters	Theory	Best fit	Difference (%)
$Z_{c,\ Bump}$ (Ω)	100	110	+10
$\varepsilon_{re,Bump}$	1	1	0
$Z_{c,\ CPW}$ (Ω)	45	40	-11
$\varepsilon_{re,CPW}$	6.95	6.9	-1
$Z_{c,\ HV}$ (Ω)	55	50	-9
$\varepsilon_{re,HV}$	12.9	12.9	0
C_{Open} (fF)	12	10	-16

B. 30-GHz Chip Scale Packaged low noise amplifier

To validate the bump-to-hot-via models, and to demonstrate potential applications of such technology, an active MMIC, re-designed for CSP mounting, with front-side BCB coating, and modified backside pattern, has been fabricated, and assembled onto a carrier substrate (medallion in Fig. 9). The MMIC device is a broadband 30-GHz low noise amplifier (LNA), exhibiting typically 15-dB gain from 15- to 30 GHz. The Fig. 9 shows a comparison between simulated, and measured S-parameters of the mounted LNA; a very good agreement is obtained up to 40 GHz, over the four S-parameters.

IV. CONCLUSION

Theoretical models, and experimental design data for the bump- to hot-via interconnects have been presented. Both are in very good agreement up to at least 110 GHz, demonstrating as well very good transition behavior, and predictable MMIC performance. The simple modeling approach in analytical forms, and transition performance, enable applications of hot-via concept to active millimeter-wave CSP ICs up- and above W-band.

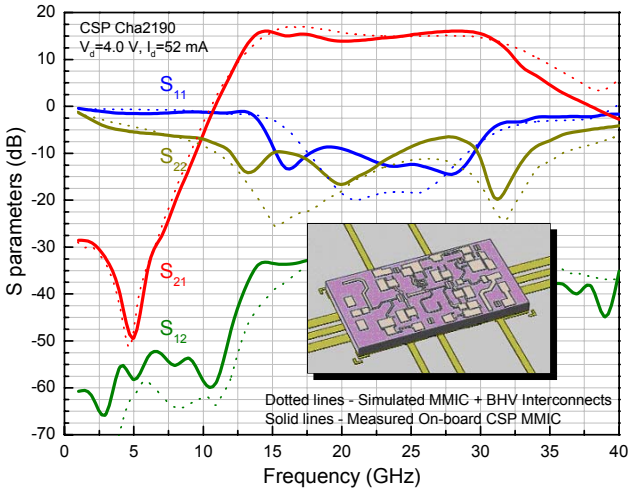

Fig. 9. Comparison between measured and simulated S-parameters of the CSP LNA with bump-to-hot-via transitions (in medallion: representation of the CSP LNA attached to its carrier test fixture).

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