Anisotropic Conductive Adhesives for Millimeter-wave Flipchip Interconnections

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***Abstract* — In this paper anisotropic conductive pastes (ACP) are proposed for the 1st level interconnect of millimeter-wave multichip modules (MCM) and packages. This 1st level interconnect between components on top of the module and the MCM is established in a flipchip approach. Here, instead of gold based bumps ACP together with a structured dielectric layer are used. The latter features additional chip support and bump shaping capabilities. These flipchip arrangements are experimentally investigated and compared to conventional gold based interconnections up to 110GHz.**

I. Motivation and Background

Multichip modules using flipchip technology as 1st level interconnect are becoming more and more popular to address the ever increasing demand for higher packaging densities at higher frequencies.

In case of multilayered modules the signal and control lines are vertically routed from these 1st level interconnects to the bottom side of the module. The 2nd level interconnect, i.e. the interconnection between the module and its motherboard, is establihed by standard surface mount technologies like ball grid arrays [1, 2].

This approach offers superior encapsulation capabilities with little influence on the electrical performance especially of the 1st level interconnect [1].

Fig. 1 shows a typical flipchip configuration. The conventional wire-bonds are replaced by gold based bumps fabricated on either the substrate or the chip. The bumps provide electrical and mechanical connection of the chip mounted upside down on the substrate. They are fabricated by a modified ball bond process (studbumps) or by gold plating [3].

In order to interconnect millimeter-wave monolithic integrated circuits (MMIC) fine-pitch dimensions are desired. These are determined by the MMIC pad dimensions. Typical pad sizes are 75µm x 75µm with a center distance (pitch) of 125µm to 150µm.

Flipchip technology meets these fine-pitch requirements and has already been proven to be a promising alternative to wire-bond interconnections up to W-band frequencies [4, 5].

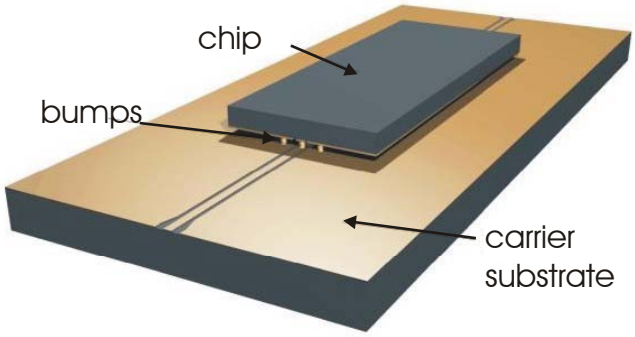

Fig. 1. Flipchip configuration with gold bumps.

Instead of studbumps conductive adhesives can be applied as well for bump fabrication up to these frequencies. Additional usage of photoresist allows bump formation and provides chip support [6].

Fig. 2 shows a corresponding test strip. In a photolithographic step small buckets are defined. These are filled by dispensing isotropic conductive adhesives for the flipchip-transition. Three buckets are needed to provide insulation between the inner and outer conductors of coplanar waveguide (CPW) lines. Because of the fine pitch the structure is very fragile.

Anisotropic conductive adhesives are well known for displays and flexible organic substrate packages [7]. They are composed of adhesive polymers filled with conductive particles. When applied between two surfaces and thermocompression bonded a permanent joint is realized.

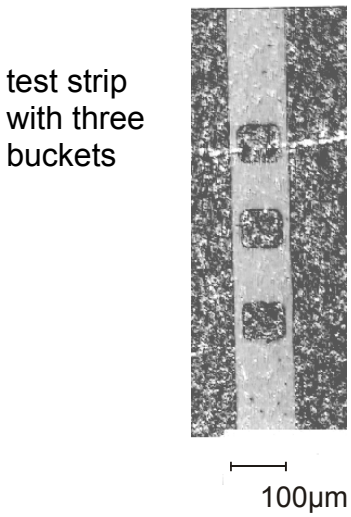

Fig. 2. Photoresist with recessed areas for isotropic conductive adhesives.

Fig. 3 illustrates the schematic side view of an anisotropic conductive adhesive cured under pressure between two substrates. Each substrate carries a CPW line. In areas where the particles are squeezed electrical conductivity is provided. Unexposed areas remain insulated. When the metallization layers are of sufficient thickness compared to the particle diameter additional bumps are not necessarily needed. These particle diameters are usually as small as 4µm to 5µm.

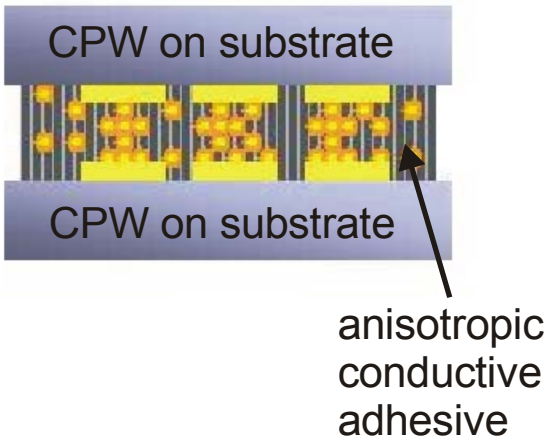

Fig. 3. Thermocompressed and cured anisotropic conductive paste interconnects two substrates.

So far, the functionality of anisotropic conductive pastes or films in electronic packages has been demonstrated up to a few GHz [8].

Here, anisotropic conductive paste is applied to millimeter-wave flipchip interconnections in a novel approach. It follows from the modified dispense technique applied to isotropic conductive adhesives in [6]. In combination with structured dielectric layers ACP builds the 1st level interconnect.

II. ACP Bump Fabrication Process

Before the ACP is dispensed photoresist is spin coated onto the carrier substrate. In a photolithographic step the photoresist is structured and open areas are defined.

Fig. 4 depicts a photoresist strip on a CPW line of the carrier substrate. It contains a recessed area that is 75µm wide and 300µm long. The photoresist layer is about 25µm thick.

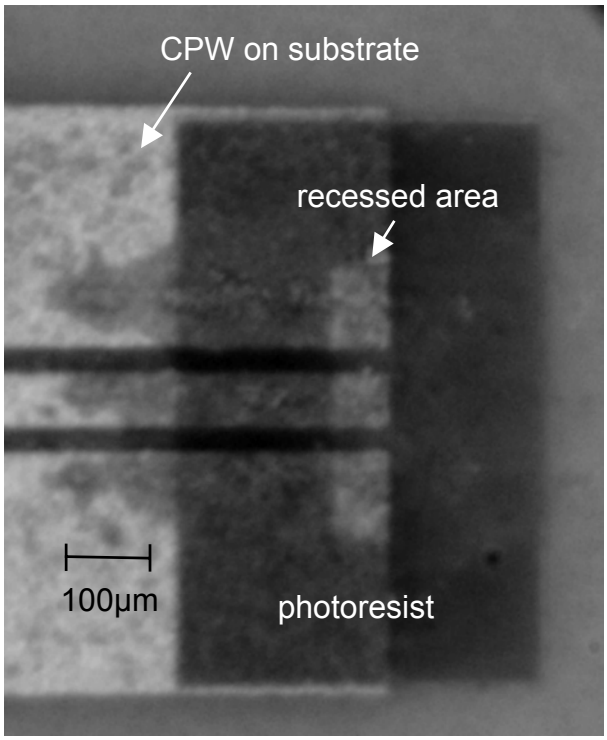

Fig. 4. Photoresist with recessed area for ACP interconnection.

Next, this area is filled with ACP in order to provide an interconnection compatible with fine-pitch flipchip technology.

For ACP a single bucket is sufficient because the insulation is provided by the anisotropic characteristics of the paste. In comparison to isotropic conductive adhesives this reduces the number of process steps and production requirements in terms of printing resolution of the photolithographic mask.

Next, complete flipchip test systems assembled following this approach are described.

III. CPW Test System

Several flipchip arrangements are fabricated. According to Fig. 1 a carrier substrate and a flipchip test device are needed.

For both components alumina substrates with a dielectric constant of 9.8 are chosen. Photolithography is applied to pattern their gold metallization layers. The flipchip devices are cut out by laser material processing.

They are 127µm-thick and comprise a 50Ω CPW line (center conductor width 38µm, ground-to-ground distance 78µm). The 254µm-thick alumina carrier substrate features 50Ω CPW lines (center conductor width 50µm, ground-to-ground distance 100µm), as well. Among them, there are through lines which serve as reference. The others exhibit a gap to be bridged by the flipchipped test devices.

Fig. 5 depicts the carrier substrate after photolithographic processing and already partly assembled with test devices. The chips have been thermocompression bonded onto the carrier after the recessed areas were filled with ACP. The reference lines can be seen at the bottom. At the edges of the substrate typical photoresist remains of the spin coating procedure are visible.

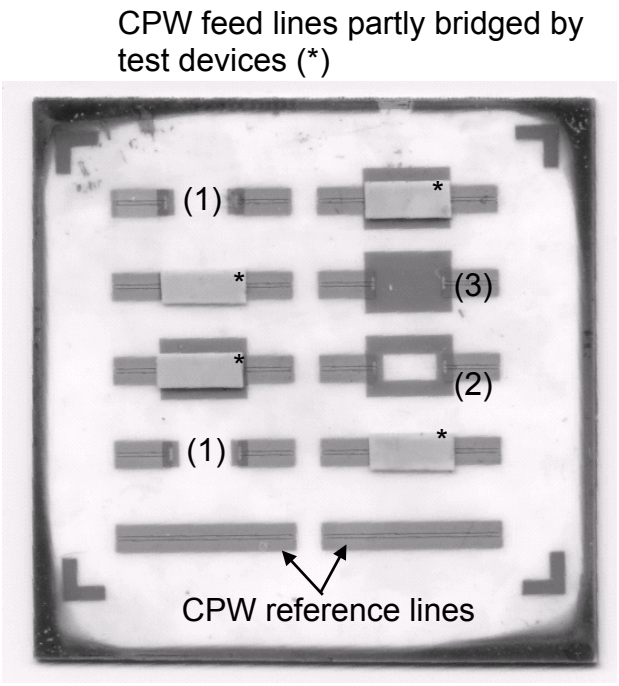

Fig. 5. Substrate with several flipchip arrangements using ACP with photoresist and studbumps.

The photoresist was patterned in three different ways as illustrated in Fig. 5.

Test structure (1) is already depicted in Fig. 4 which shows an enlarged view of the left flipchip contact. Type (2) exhibits photoresist that forms a ring to support the test device. The photoresist is removed from critical areas underneath the chip. The side areas are expected to have negligible impact on the electrical performance of the test device. Type (3) fully underfills the test device.

Besides the ACP flipchip arrangements conventional studbumped interconnections are considered as well for comparison. These gold interconnections are produced using an altered ball bonding process, where the gold wire is cut after the first bump has been set. Three gold balls of 70µm-diameter and a 150µm-pitch build a CPW-transition. The complete flipchip arrangement has six such metallic bumps. The test device is connected by thermocompression bonding.

IV. Measurement Results

The test systems are characterized by means of a vector network analyzer (VNA) and a probe station with CPW tips (100µm-pitch) in a single sweep up to 110GHz.

In Fig. 6 the measured transmission $|S_{21}|$ and input reflection $|S_{11}|$ are presented for both ACP and studbumped flipchip arrangements as well as the CPW reference line.

The ACP flipchip arrangement consisting of two CPW feed lines on the carrier substrate, a CPW test chip, and two ACP interconnections with photoresist strips according to Fig. 4 shows good electrical performance over the complete frequency band as compared to the studbumped interconnections. For both flipchip approaches the input reflection of the back-to-back arrangement essentially remains below -10dB up to 110GHz.

Compared to the CPW reference line, i.e. without flipchipped device, the transmission loss of the ACP arrangement is only increased by 1dB (1.5dB) up to 100GHz (110GHz).

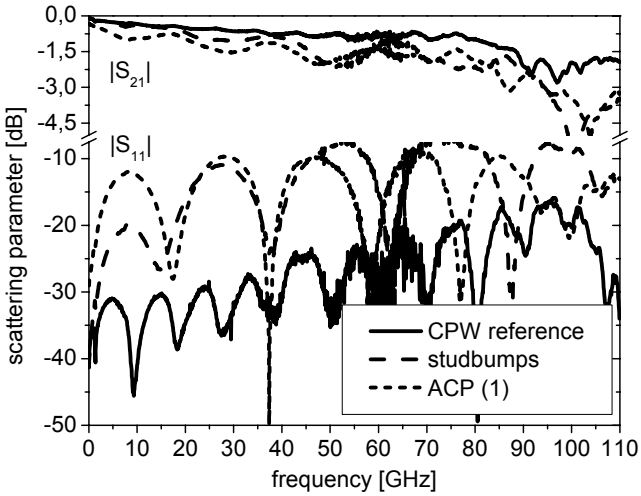

Fig. 6. Measured scattering parameters of ACP flipchip arrangement (1) and reference lines.

Thus, the transmission loss per single ACP flipchip transition remains below 0.5dB (0.75dB) up to 100GHz (110GHz).

Fig. 7 depicts the measurements for the three different ACP arrangements labelled according to Fig. 5. Only slight differences in the measured scattering parameters are observed. They can be related to manufacturing tolerances and the influence of the underfill on the electrical properties, both effects being obviously very small. This underlines the easy handling and good reproducibility of this technological approach.

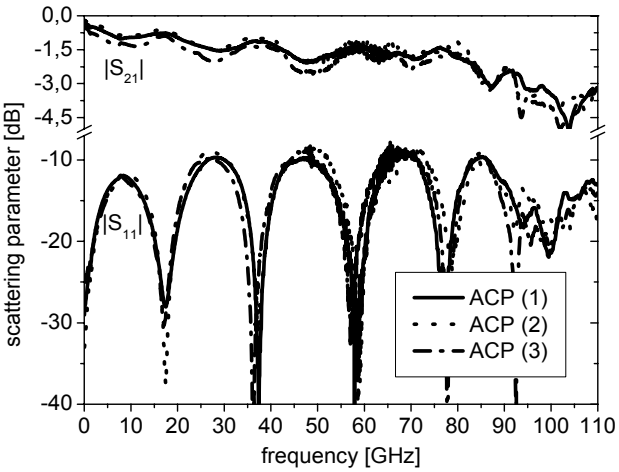

Fig. 7. Measured scattering parameters of ACP flip-chip arrangements up to 110GHz.

V. CONCLUSION

This paper reports on novel millimeter-wave flipchip interconnections. Anisotropic conductive paste (ACP) and a structured dielectric layer are applied. The latter features bump formation in terms of bump shape and height as well as chip support. The anisotropic conductive characteristic of the adhesive reduces the assembly efforts and the complexity of the flipchip joint. Compared to conventional studbumped interconnections these ACP flipchip arrangements show competitive electrical performance up to 110GHz. So far, this technological approach has been successfully applied to 1st level flip-chip interconnections. Ongoing work is devoted to the application of ACP to novel millimeter-wave package solutions.

REFERENCES

[1] J. Heyen, T. v. Kerssenbrock, A. Chernyakov, P. Heide, A. F. Jacob, “Novel LTCC-/BGA-Modules for Highly Integrated Millimeter-Wave Transceivers”, *IEEE Trans. Microwave Theory Tech.,* vol. 51, no. 12, Dec. 2003, pp. 2589-2596.

[2] J. Heyen, A. Gordiyenko, P. Heide, A. F. Jacob, “Vertical Feedthroughs for Millimeter-Wave LTCC Modules”, *Proc. 33rd EuMC 2003,* Munich, Oct. 2003, pp. 411-414.

[3] J. H. Lau, *Flip chip technologies*, New York: Mc Graw-Hill, 1996.

[4] H. Kusamitsu, Y. Morishita, K. Maruhashi, M. Ito, K. Ohata, "The Flip-Chip Bump Interconnection for Millimeter-Wave GaAs MMIC," *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 22, no. 1, pp. 23-28, January 1999.

[5] W. Heinrich, A. Jentzsch, G. Baumann, "Millimeter-Wave Characteristics of Flip-Chip Interconnects for Multi Chip Modules," *IEEE Trans. Microwave Theory and Tech.*, vol. 46, no. 12, pp. 2264-2268, December 1998.

[6] J. Heyen, J. Schroeder, A. F. Jacob, "Low-Cost Flip-Chip Alternatives for Millimeter Wave Applications," *IEEE MTT-S International Microwave Symposium Digest*, pp. 2205-2208, June 2002.

[7] H. Kristiansen, J. Liu, "Overview of Conductive Adhesive Interconnection Technologies for LCD’s," *IEEE Transactions on Components, Packaging, and Manufacturing Technology – Part A.*, vol. 21, no. 2, pp. 208-214, June 1998.

[8] M.-J. Yim, W. Ryu, Y.-D- Jeon, J. Lee, S. Ahn, J. Kim, K.-W- Paik, "Microwave Model of Anisotropic Conductive Film Flip-Chip Interconnections for High Frequency Applications," *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 22, no. 4, pp. 575-581, December 1999.