Low Noise Amplifiers for 94 GHz Cloud Radar

Mikko Kärkkäinen[1], Mikko Varonen[1], Mikko Kantanen[2],
Timo Karttaavi[2], Pekka Kangaslahti[1] and Kari Halonen[1]

[1]Helsinki University of Technology, Electronic Circuit Design Laboratory,
Espoo, P.O. Box 3000, FI-02015 HUT, Finland, Tel. +358 9 451 2276
[2] Technical Research Center of Finland (VTT Information Technology),
P.O. Box 1202, FI-02044 VTT, Finland

Abstract — **Four low noise amplifiers for 94 GHz cloud radar are presented. One LNA is designed using coplanar waveguides and the others use microstrip lines. The designed amplifiers were manufactured with a metamorphic high electron mobility transistor (MHEMT) technology and the chip size is 2.1 mm x 1.1 mm. The four stage LNAs have either 2x25 µm or 4x25 µm size MHEMTs. The scattering parameters and the noise figures of the amplifiers were measured at W-band and the results are presented. The best measured gain at 94 GHz was 16 dB and the noise figure 5.7 dB using a 2.5 V supply voltage and a drain current of 15 mA per stage. Furthermore, one of the amplifiers was assembled in a package that has WR-10 waveguide interfaces. The packaged chip exhibited 10.8 dB of gain and the noise figure was 8 dB at 94 GHz.**

I. Introduction

We present measurement results obtained from our integrated low noise amplifier circuits fabricated by OMMIC, France using metamorphic HEMT (high electron mobility transistor) technology. This activity in general aims at developing a receiver for the 94 GHz Cloud Profiling Radar (CPR), a candidate instrument for the EarthCARE (Earth Clouds, Aerosols and Radiation Explorer) mission of the European Space Agency (ESA) [1]. The purpose of our project was to see how well the metamorphic technology suits to the 94 GHz low noise amplification.

II. Manufacturing Technology

In MHEMT technology a metamorphic buffer layer is grown on the GaAs, which enables the growth of a channel layer having 30-80 % indium content. This way it is possible to combine some of the good properties of purely indium phosphide or gallium arsenide based processes. High indium content provides more gain and less noise, but low indium content is suitable for high breakdown applications such as power amplifiers [2]. The chosen process features 0.15 µm metamorphic HEMT devices and the transistor f_t is around 150 GHz.

III. Low Noise Amplifier Design

Since there was no noise model provided by the foundry, we obtained some test transistors for accurate noise characterisation purposes. The noise parameters of the transistor were measured at W-band and the noise data was used in the simulations. The noise parameters were measured using methods that are described in [3]. The noise parameters of the transistor were simulated by using a temperature noise model that is described in [4]. The temperature of the drain-to-source resistance was raised to 2227 K. The simulated and measured noise parameters of a 4x25µm MHEMT are presented in Figs. 1-3. The noise resistance has the largest deviation from the measured values, but all the other parameters have a good match. The small transistor was not available for testing during the LNA design.

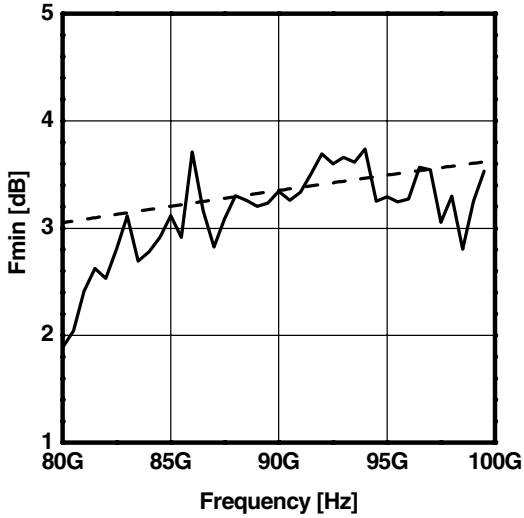

Fig. 1. Measured and simulated (dashed line) minimum noise figure of a 4x25µm MHEMT.

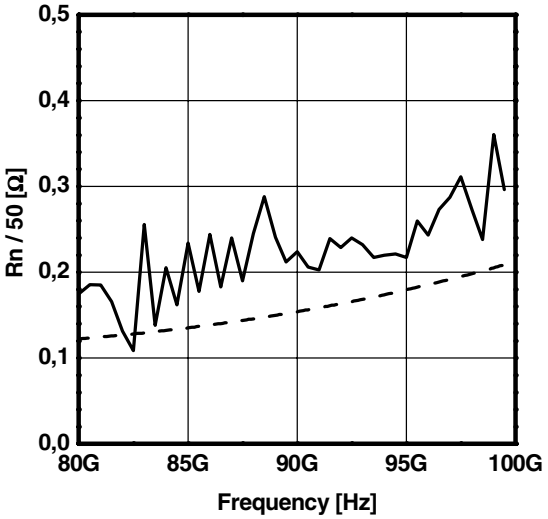

Fig. 2. Measured and simulated (dashed line) normalised noise resistance of a 4x25µm MHEMT.

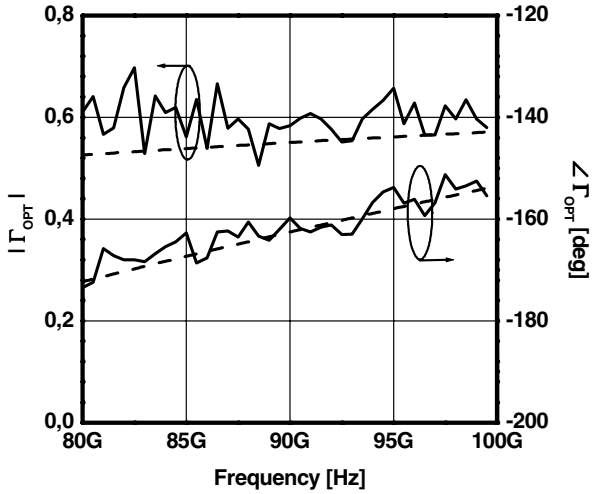

Fig. 3. Measured and simulated (dashed line) optimum reflection coefficient of a 4x25µm MHEMT.

A set of four LNA designs consists of three microstrip amplifiers and one coplanar waveguide (CPW) design LNA3. Two amplifiers, LNA2 and LNA4, were designed using 4x25 µm MHEMTs and all the others use 2x25 µm transistors. Every LNA has four stages and the chip size is 2.1 mm x 1.1 mm. The photographs of the fabricated LNA1 and LNA3 chips are presented in Fig. 4 and Fig. 5, respectively. Finally, one of the amplifiers was assembled in a split block package, which has WR-10 waveguide interfaces with alumina transitions.

The matching networks consist of on-chip series transmission lines and shunt stubs. For example, the input of the LNA1 is matched with an open shunt stub and the output with a short-circuited shunt stub, which is also used for drain biasing. The stub is short circuited with a 50 fF metal-insulator-metal(MIM)-capacitor and a ground-VIA-hole. The capacitor forms a resonance circuit with the series inductance of the VIA-hole at the design frequency. This is a low impedance point, which makes the DC-connections as invisible as possible at RF-frequency. The gate bias is inserted through a quarter-wave shunt stub, which has a similar short-circuit structure. However, in the coplanar waveguide design (LNA3) the capacitance of the short-circuit capacitor is increased to 100 fF, because of the presumably better grounding. The biasing networks are stabilized with 32-40 Ohm resistances at gates and drains. In addition, 4 pF shunt capacitors are used between the resistances to provide out-of-band stability and large 8-15 pF capacitors are connected to drain voltage feed lines in order to improve supply stabilization.

The source ground vias are located nearby the transistor since the available gain is low for a single stage and any addition of feedback would cause degradation of performance. The exact separation of the source ground vias is defined by the design rules.

In case of the coplanar design (LNA3) the bias network was drawn with microstrip lines, but the RF parts utilize conductor backed coplanar waveguides. The unwanted slotline mode is suppressed by placing airbridges around discontinuities [5]. Because of the relatively thin substrate and limited ground plane width, the parasitic microstrip mode can be present. Vias are used for connecting the ground planes on the surface to zero potential to further reduce the possibility of propagating unwanted modes [6]. In addition, good grounding decreases the feedback that is caused by microstrip lines at transistor sources in the other designs.

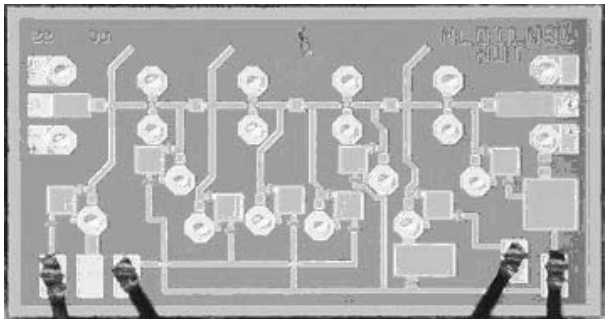

Fig. 4. Photograph of the LNA1 chip.

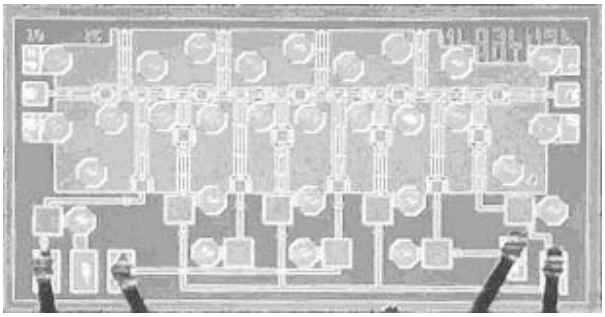

Fig. 5. Photograph of the LNA3 chip.

TABLE I
MEASURED PERFORMANCE AT 94 GHZ.

	MHEMT size	Gain [dB]	NF [dB]	V_{supply} [V]	Total drain current [mA]	DC Power [mW]
LNA1	2x25 µm	12.7	6.8	2.2	40	88
LNA2	4x25 µm	16.3	5.7	2.5	60	150
LNA3 (CPW)	4x25 µm	12.6	7.5	2.0	50	100
LNA4	4x25 µm	14.1	6.8	2.5	62	155
Packaged LNA1	2x25 µm	10.8	8.0	2.0	40	80

IV. Measurement Results

The scattering parameters and the noise figures of the amplifiers were measured on-wafer at W-band with coplanar probes. The measured results are presented in figures 6-9. The gain varies between 12.6 and 16.3 dB and the noise figure is between 5.7 and 7.5 dB at 94 GHz.

The first version (LNA1) was assembled in a split block package that has WR-10 waveguide interfaces. A photograph of the packaged LNA1 chip is presented in Fig. 10 and the measurement results are in Fig. 11. The gain of the packaged amplifier drops more rapidly after 90 GHz, but we still have 10.8 dB gain at 94 GHz. The noise figure rises significantly at 94 GHz, but, on the other hand, we have better gain and lower noise between 85 and 90 GHz

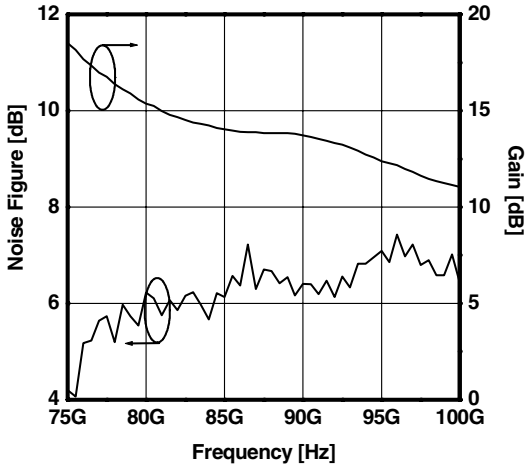

Fig. 6. Measured gain and noise figure of the LNA1.

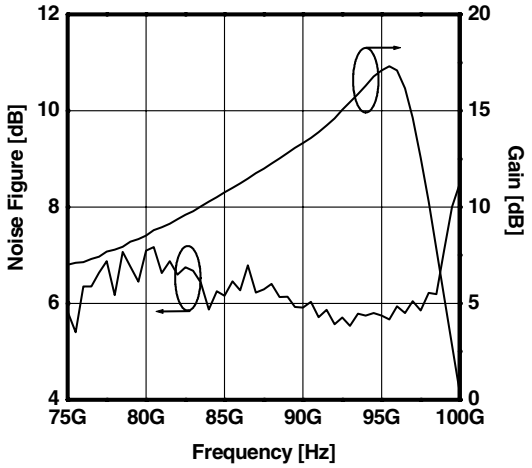

Fig. 7. Measured gain and noise figure of the LNA2.

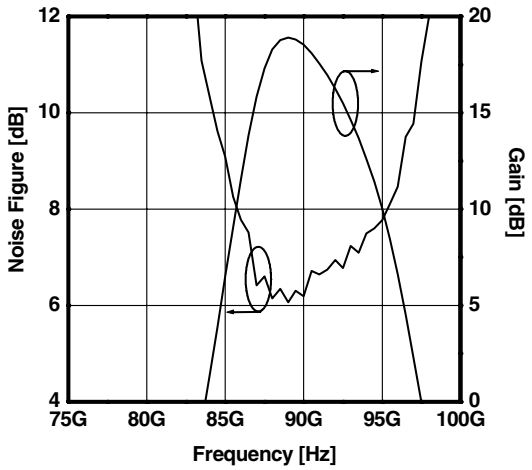

Fig. 8. Measured gain and noise figure of the LNA3.

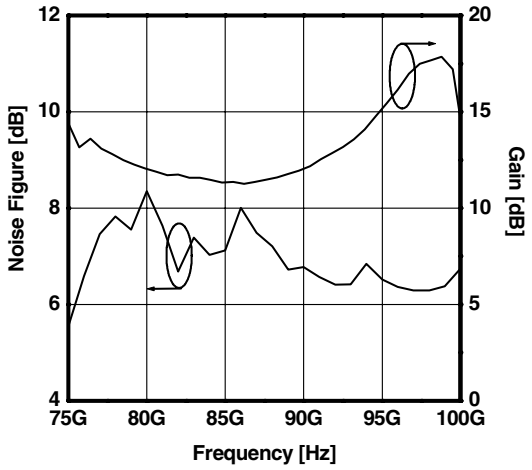

Fig. 9. Measured gain and noise figure of the LNA4.

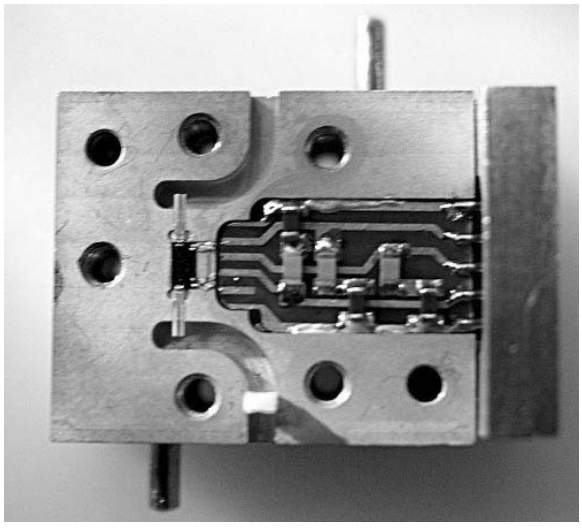

Fig. 10. Photograph of the packaged LNA1 chip.

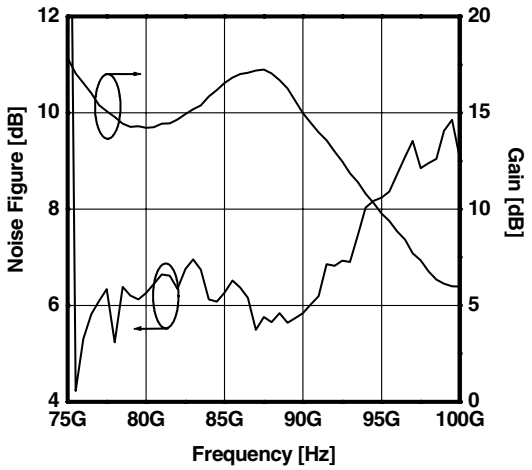

Fig. 11. Measured gain and noise figure of the packaged LNA1 chip.

VI. Conclusion

The measured performance of the 94 GHz low noise amplifiers is gathered in Table I. The achieved noise figure of 5.7 dB and gain of 16.3 dB for the LNA2 were the best measured results at 94 GHz. The coplanar version (LNA3) has a good gain curve that is concentrated around 85-95 GHz. If its center frequency had been correct (94 GHz), its performance would have been comparable with LNA2. The best measured results for the coplanar version were achieved at 89 GHz. The measured gain is 18.9 dB and the noise figure is 6.1 dB.

In case of the packaged chip the gain is 1.9 dB lower and the noise figure is 1.2 dB higher when compared to the on-wafer measurement results.

Acknowledgement

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