High-Performance CMOS-Compatible Micromachined Edge-Suspended Coplanar Waveguides on Low-Resistivity Silicon Substrate

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***Abstract* — This paper reports a novel low-loss CMOS-compatible coplanar waveguide (CPW) structure based on the micromachined edge-suspension of the signal line. It is revealed that, at radio or microwave frequencies, the current is highly concentrated along the edges of the signal line. Since the coupling to the low resistivity silicon substrate is dominated by the current carrying part, the substrate coupling and loss can be effectively suppressed by removing the silicon along and underneath the edges of the signal lines. The edge-suspended structure has been implemented by a combination of deep reactive ion etching and anisotropic wet etching. The suspended structure shows much reduced loss (0.5 dB/mm at 39 GHz) and strong mechanical strength that is provided by the silicon underneath the center of the signal line.**

I. INTRODUCTION

With the rapid development in wireless and portable communication, there is an increasing demand for low-cost and miniaturized radio-frequency (RF) and microwave monolithic integrated circuits. While the active transistors have experienced steady enhancement in device performance as a result of the advancing CMOS technology, it is still challenging to realize low-loss high-frequency passive components including coplanar waveguides (CPWs) on standard CMOS-grade silicon substrates, which normally have low resistivity in the range of 1–20 Ω-cm. Significant loss can be generated at microwave frequencies as a result of the signal coupling into the low-resistivity silicon substrate. In order to overcome this dominant loss factor in silicon-based microwave passive components, different approaches have been investigated. Firstly, high resistivity silicon (HRS) [1] (ρ > 2500 Ω-cm) can be used to reduce the substrate loss. Proton implantation can also be used to convert low resistivity silicon to high resistivity silicon [2]. However, RF and microwave integrated circuits are usually fabricated on low-cost low-resistivity silicon using standard CMOS production process. Secondly, the substrate coupling can also be effectively reduced by inserting a low-loss low-k dielectric layer [3]–[4] between the CPW and the lossy silicon substrate. Another widely investigated approach is to apply micromachining techniques to remove the silicon substrate underneath (or around) the signal line to reduce the substrate loss [5]–[6].

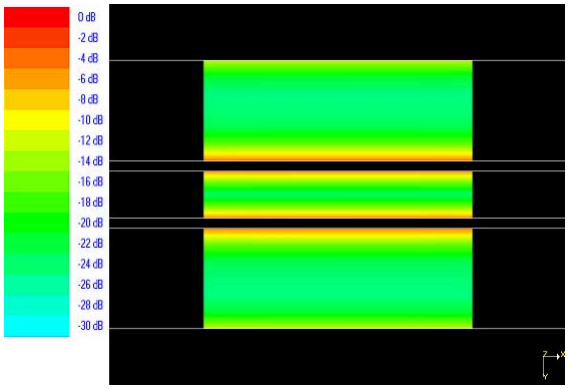
However, the CPWs fabricated on the suspended membrane require sophisticated backside processing and their mechanical strength is also questionable, especially for long CPWs. The micromachined overlay CPW structure by Kim et al. [7] also requires the airbridge technique and it remains to be seen whether it can be compatible with the standard CMOS process. Herrick et al. [8] implemented CPWs with etched groves around the signal line in CPW to reduce the line capacitance, and the approach is CMOS compatible.

In this paper, we propose and demonstrate a novel micromachined edge-suspended CPW (ESCPW) structure that features the removal of silicon substrate around and underneath the edge of the signal (and ground) lines. At RF and microwave frequency range, the substrate coupling is dominated by the region located between the signal and ground lines, and *the region under the edge of the line*. Since the edge is the location where the current is concentrated (current crowding) due to proximity effect, removing the silicon under the edge can effectively reduce the line capacitance and the substrate loss. We obtain a loss of 0.5 dB/mm at 39 GHz for a CPW that use CMOS-compatible 1 μm thick aluminum (Al) metal. Only an inductively coupled plasma deep reactive ion etching (ICP-DRIE) and anisotropic silicon wet etching are added to the standard CMOS process, and the process is CMOS-compatible. In addition, silicon beneath the center of the signal line is left untouched to provide strong mechanical support. Three-dimensional finite-difference time-domain (FDTD) simulation is also presented to show the current and electric field distribution along the CPW and ESCPW.

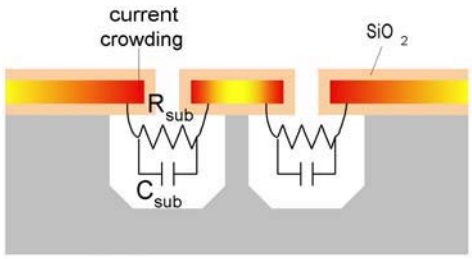
II. OPERATING PRINCIPLE OF EDGE-SUSPENDED CPW

The concept of the edge suspended CPW is illustrated in Fig. 1. At DC and low frequencies, the current is uniformly distributed. As frequency increases, with the skin effect and proximity effect becoming significant, the AC current is pushed towards the edges of signal line, resulting in an uneven current distribution. The current distribution of a conventional CPW operating at 10 GHz is simulated with the EM simulator, IE3D and is shown in Fig. 1(a). Most of

the current is concentrated along the two edges of the signal line. The current carrying portion of the line dominates the signal-to-ground coupling which is through the air above the CPW plane and the substrate below the CPW plane. The substrate coupling, if not suppressed, can lead to significant amount of loss in the low resistivity silicon substrate, degrading the loss performance of the silicon-based CPWs. We propose to utilize micromachining techniques to create an edge-suspended CPW (ESCPW) structure as shown in Fig. 1(b). By removing the silicon not only in the region between the signal and ground, but also the silicon under the edges of the signal and ground lines, substrate coupling is expected to be suppressed significantly, leading to great reduction of loss in the ESCPW.



(a)



(b)

Fig. 1: (a) Simulated current distribution in a conventional CPW operating at 10 GHz; (b) Cross-sectional view showing the current distribution in the ESCPW with reduced substrate coupling.

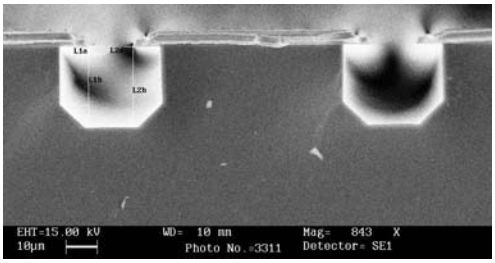
	S (in μm)	W (in μm)
CPW1	8	30
CPW2	10	40
CPW3	11	50
CPW4	18	70
CPW5	20	70

Table I: Physical dimensions of various CPW design.

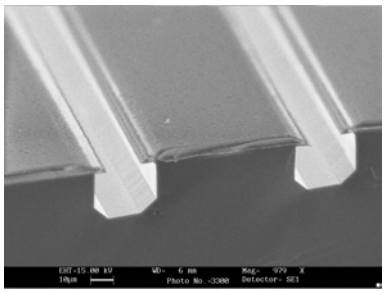
III. Fabrication of Edge-Suspended CPW

The ESCPWs with different physical dimensions as shown in Table I were fabricated on standard CMOS-grade (100) silicon substrates with a resistivity of 20 Ω-cm. Aluminum of 1 μm was used as the signal and ground metal. Etching windows were first patterned between the signal and ground lines. Silicon oxide passivation layer in the etching windows is removed by RIE. ICP-DRIE was used to create the trenches around the conducting wires.

An anisotropic etching solution of 5 wt% tetramethyl ammonium hydroxide (TMAH) mixed with 0.5 wt% $(NH_4)_2S_2O_8$ and dissolved silicon [9] is used to create the lateral undercut along the <100> direction. This etching solution selectively etches the {100} and {110} Si crystal planes, but not the {111} plane. The use of TMAH solution for etching of silicon is CMOS-compatible as it has no mobile K+ contamination issue that is often encountered in the KOH-like etchant. This etchant also has negligible etching of aluminum. A cross-sectional view of an ESCPW viewing at different angles: 90° and 80° after TMAH etching (with an undercut of 8 μm) are shown in Fig. 2(a) and (b) respectively. In the layout design of the ESCPWs, the CPWs must be aligned in such a way that the lines are in 45-degree angle with the major cut (<110> direction) of a (100) silicon wafer. It was found that if the lines are aligned or perpendicular to the major cut of the wafer, minimum undercut will be created since the {111} plane will be exposed quickly during the TMAH etching and the etching stops at the {111} plane.



(a)



(b)

Fig. 2: SEM images of the ESCPW with different viewing angle: (a) 90° and (b) 80°.

IV. Results and Discussions

CPWs with a nominal characteristics impedance of 50 Ω with different line width (*W*) and spacing (*S*) have been designed, with design parameters given in Table I. Vertical etching trenches *(DRIE)* were created by ICP-DRIE to either 15-μm or 30-μm deep. Then, CPWs with different lateral undercut *(UC)* were fabricated by controlling the

time of TMAH anisotropic etching as shown in Fig. 3. Undercuts of 0, 5, 8, 11, 14 µm were obtained. On-wafer S-parameter was measured using Agilent 8722E network analyzer and Cascade microwave ground-signal-ground (GSG) probes from 0.1 to 40 GHz.

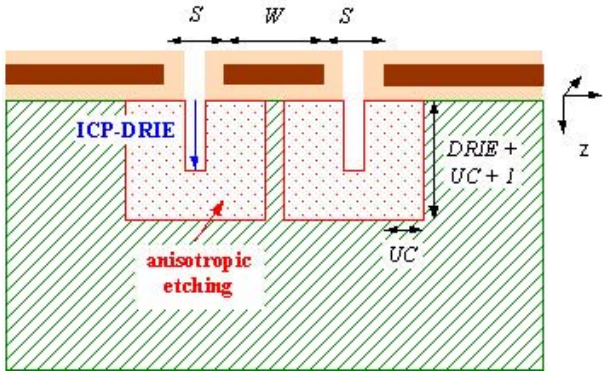


Fig. 3: Cross-sectional view of the edge-suspended CPW (ESCPW).

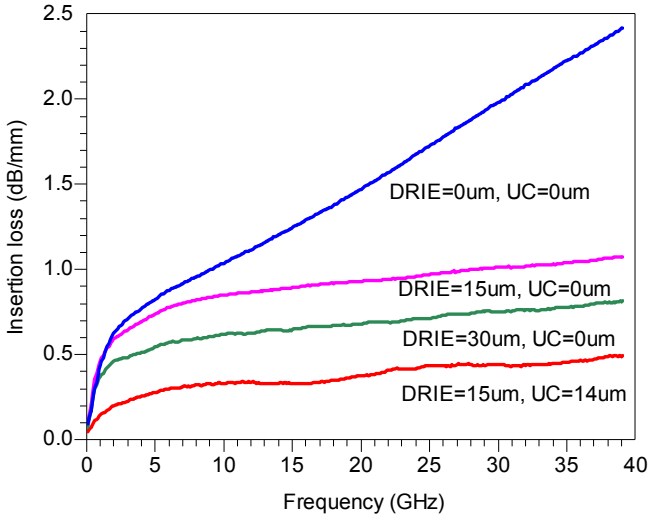


Fig. 4: Performance comparison of the narrowest CPW (CPW1) with different trench depth created by ICP-DRIE (DRIE) and undercut length (UC) created by anisotropic etching.

The performance of the CPWs with different trench depth created by ICP-DRIE and undercut created by anisotropic etching is compared in Fig. 4. When a vertical trench of 15 µm (DRIE = 15 µm) is created yet no undercut is formed (UC = 0 µm), the insertion loss of the CPWs is greatly reduced by 1.4 dB/mm since the substrate coupling in the region between signal and ground is suppressed by the removal of the silicon. As the depth of the trench increases, the loss decreases. Nevertheless, the effect becomes less prominent as the depth increases since the E-field coupled decreases in z-direction as shown in Fig. 5. To further suppress the loss through substrate coupling along the edges of the lines, undercut is created. After a 15-µm trench *(DRIE)* and 14-µm undercut *(UC)* are formed by ICP-DRIE and anisotropic etching respectively (DRIE = 15 µm, UC = 14 µm), the loss can be further suppressed by 0.4 dB/mm.

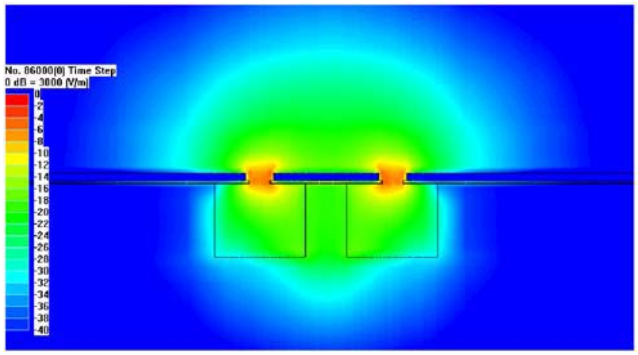


Fig. 5: Simulated E-field distribution in an ESCPW operating at 2 GHz.

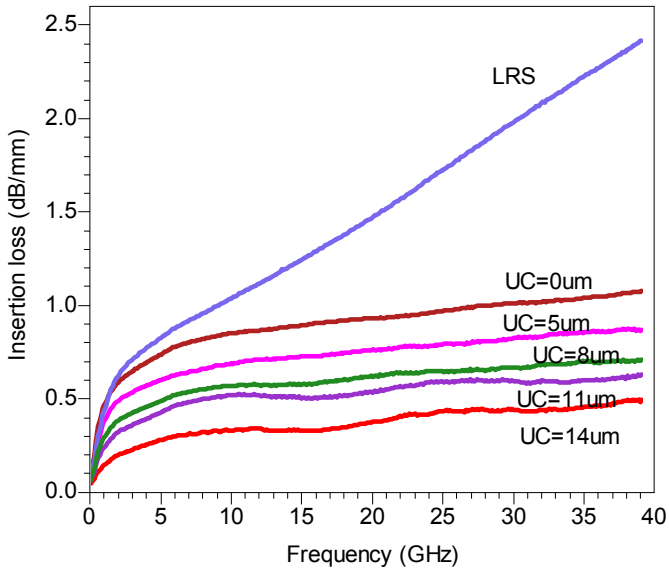


Fig. 6: Performance comparison of CPW1 with different degree of undercut length (UC) after a 15-µm trench is formed by ICP-DRIE.

Fig. 6 plots the insertion loss of the narrowest CPW (CPW1) with different degree of undercut after a 15-µm trench is formed by ICP-DRIE. The more is the undercut, the lower is the loss. With an undercut of 14 µm, the insertion loss can be reduced to 0.5 dB/mm at 39 GHz. To evaluate the effect of the physical dimensions on the CPW's performance, the insertion loss of the CPWs with 14-µm undercut but physical dimensions shown in Table I is compared in Fig. 7. The insertion loss decreases with the physical dimensions. This trend is opposite to what is observed in CPWs on insulating material. As electric field will be coupled to ground through the shortest path, in the presence of the low resistivity silicon substrate, the electric field is coupled to the supporting silicon substrate underneath the center of the CPW. Hence, with the same undercut, the wider is the CPWs, the more the electric field will be coupled to the supporting substrate and the higher is the loss. In order to further reduce the loss, wider CPWs with deeper undercut should be used.

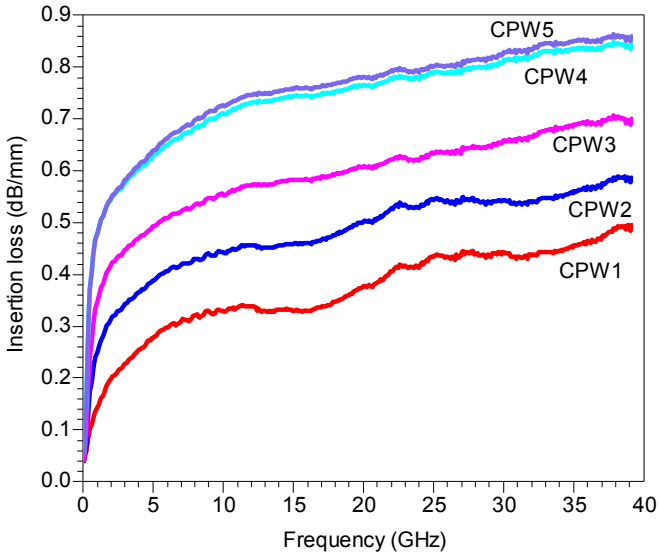


Fig. 7: Performance comparison of the CPWs with 14-μm undercut but different physical dimensions shown in Table I.

V. Conclusion

A novel edge-suspended CPW structure was demonstrated using CMOS-compatible fabrication process. Edge-suspended CPWs using CMOS-standard aluminum metal can achieved insertion loss as low as 0.5 dB/mm at 39 GHz on low-resistivity silicon substrate. With deeper vertical trench and implementation of high conductivity metal (such as copper), the edge-suspended CPWs are expected to provide even smaller insertion loss. An important advantage of the edge-suspended CPWs is that the ESCPWs possess strong mechanical support and reliability.

Acknowledgement

This work was supported in part by the Hong Kong Government Research Grant Council under Grant HKUST6173/02E, and in part by the Institute of Integrated Micro-Systems of HKUST under Grant I2MS01/02.EG05.

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