A 22-GHz Ultra Low Phase Noise Push-Push Dielectric Resonator Oscillator Using MMICs

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***Abstract* — In this paper, we present a 22-GHz ultra low phase noise push-push dielectric resonator oscillator (DRO) using MMICs fabricated by 2-μm GaAs HBT process. This circuit demonstrated a low phase noise of -114 dBc/Hz and -134 dBc/Hz at offset frequency of 100 kHz and 1 MHz, respectively. The second harmonic output power is above 6 dBm with a fundamental suppression of over 30 dBc. This DRO exhibits good phase noise performance based on the figure-of-merit carrier frequency, offset frequency, and dc power compared with the reported push-push DRO, which is due to low 1/*f* noise HBT and reproducible MMIC chips. In addition, this is the first reported push-push DRO implemented using MMICs.**

I. INTRODUCTION

Low phase noise oscillators are essential for high speed wireless digital communication systems, especially for fixed wireless access, high definition TV transmission, and broadband wireless access systems [1]-[2]. For modern communications, high-level digital modulations, such as M-QAM, are frequently used to enhance the frequency efficiency and transmission data rate [3]. Typical phase noise requirements of local oscillator (LO) for the 64-QAM modulation are better than -90 and -110 dBc/Hz at offset frequency of 10 kHz and 100 kHz, respectively [4]. Therefore, DRO is appropriate for these applications due to its excellent spectral purity and low phase noise.

The oscillation frequency of a DRO can be promoted by using the push-push oscillator approach, with the low phase noise property preserved. A number of push-push DROs implemented with hybrid MICs were reported in [5]-[8]. Since the symmetry of two oscillators in push-push DRO will influence the fundamental suppression [8], we utilized to use MMICs for the push-push DRO design to take advantage of the reproducibility of the MMIC chips. From the circuit simulations, we can see that the phase noise and the suppression are strongly related to the most imbalances, such as device characteristics, matching networks, and power consumptions.

The phase noise performance of a oscillator can be evaluated by the FoM including phase noise $L(\Delta f)$, carrier frequency f_c, offset frequency Δf, and total dc power consumption P_{DC} [9], as

$$FoM = 10\log\left[(f_c/\Delta f)^2/\left(L(\Delta f)P_{DC}\right)\right] \qquad (1)$$

Table I summarized the features and performances of the reported push-push DROs. Our circuit exhibits an RF output power of 6 dBm, a fundamental suppression of 30 dB, and a phase noise of -114 and -134 dBc/Hz at offset frequency of 100 kHz and 1 MHz, respectively with the best phase noise FoM of 197 dB.

II. CIRCUIT DESIGN

The schematic of the push-push DRO is shown in Fig. 1, which comprises two identical MMIC oscillator chip to provide negative resistances, a KYOCERA 11-GHz dielectric resonator, and microstrip/coupler lines on 8-mil Duriod substrate. The equivalent circuit of the dielectric resonator with two couplers is a parallel R-L-C circuit and two ideal transformers with turn ratios of 1:1 and 1:-1 [4]. The MMICs are designed, using 6" GaAs 2-μm HBT MMIC process provided by WIN Semiconductors. The two-emitter-finger device with a total emitter size of $2 \times 2 \times 20$ μm^2 is selected for the oscillator design. This device exhibits a typical collector-to-emitter breakdown voltage of 13 V, maximum collector current of 48 mA, unit current gain frequency f_T of 36 GHz and maximum oscillation frequency f_{max} of greater than 135 GHz at 3.6-V collector voltage [10].

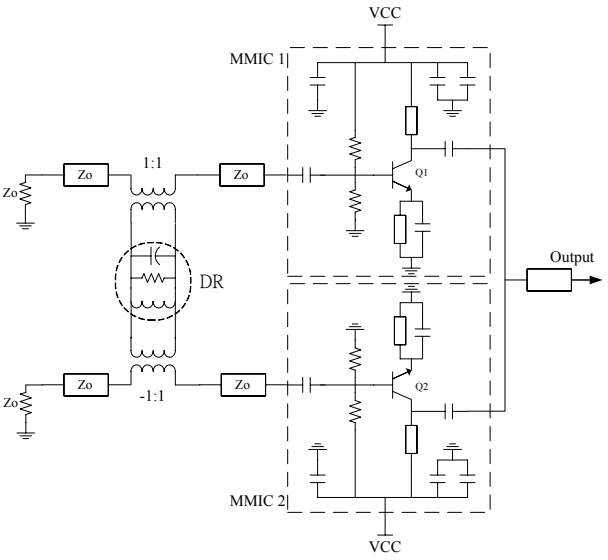

Fig. 1. Schematic of the push-push DRO..

Fig. 2 is the microphotograph of MMIC oscillator chip with chip size of 1×1 mm^2. The function of the MMIC is to provide negative resistance for the DRO, which employs a common-emitter HBT. The positive feedback is achieved with a transmission line at the emitter, and thus produces the negative resistance looking into the base. The dc blocking in the input/output is accomplished with the matching metal-insulator-metal (MIM) capacitors. The MIM capacitors are also used for RF bypass in the biasing networks.

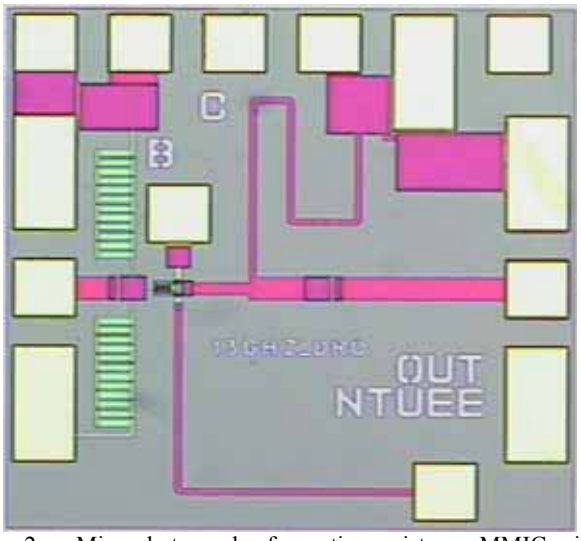

Fig. 2. Microphotograph of negative-resistance MMIC with a chip size of 1×1 mm^2.

The HBT Gummel Poon model provided by WIN Semiconductors is used for the circuit simulation. The transmission lines and MIM capacitors are simulated and verified using the full-wave EM-simulator. The complete circuits are simulated using Agilent ADS circuit design software, and the simulated second harmonic output power is about 10 dBm

III. Measurement Results

The *S*-parameters measurements of the MMICs were performed via on-wafer probing using Agilent 8510C network analyzer. Ten MMICs have been measured and the *S*-parameters are almost identical. The measured return gains between 8 and 22 GHz are plotted in Fig. 3. The measured return gain is greater than 2 dB between 10 and 16 GHz, at the collector voltage of 3.3 V with collector current of 12 mA.

The MMIC chips were then assembled in packaged module with a SMA connector for fundamental frequency DRO and push-push DRO measurement. The photograph of the push-push DRO module is shown in Fig. 4. The output spectrum of the DROs was measured using Agilent 8565EC spectrum analyzer. The measured output spectrum of the push-push DRO is plotted in Fig. 5. The measured second harmonic output power is 6 dBm at 21.9 GHz, while the fundamental suppression is better than 30 dB (corrected with the cable loss). Another module was assembled for the single DRO measurement, which used only one MMIC chip. The fundamental output power is about 10 dBm with a frequency of 10.9 GHz. The total dc power consumption is about 132 mW (3.3 V $\times$ 40 mA) for one MMIC in push-push operation.

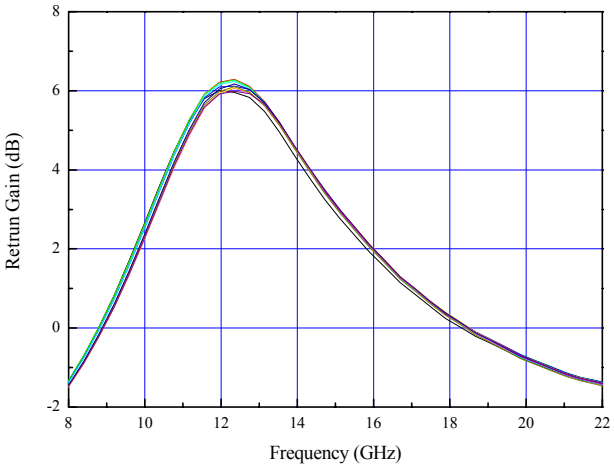

Fig. 3. Measured return gains of ten negative-resistance MMICs between 8 and 22 GHz.

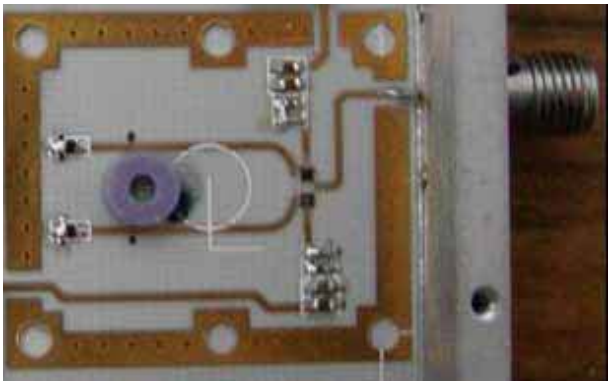

Fig. 4. Photograph of the push-push DRO module.

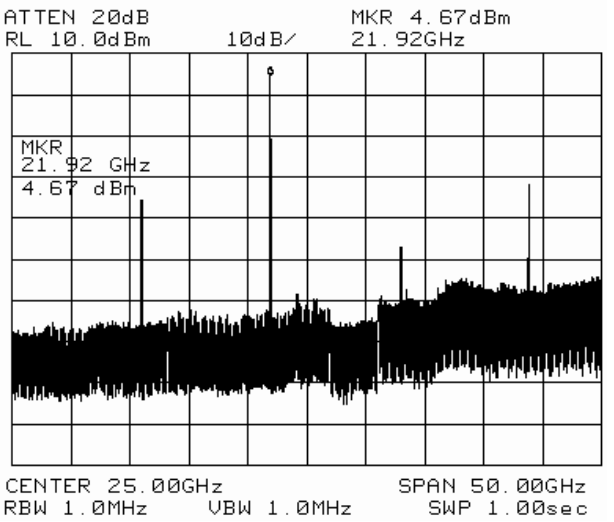

Fig. 5. Measured output spectrum of push-push DRO with a RF output power of 6 dBm.

The phase noise measurements for the DROs were evaluated using Agilent E5504A dedicated phase noise test set. An Agilent 8662A signal generator was used as the reference source for the phase noise measurements, which was phase locked to the under test oscillator in direct-current frequency-modulation (DCFM) mode. The measured phase noise is plotted in Fig. 6 for the fundamental and second harmonic of push-push DRO against offset frequency from 1 kHz to 4 MHz, which presents a phase noise of -114 dBc/Hz and -134 dBc/Hz at offset frequency 100 kHz and 1 MHz respectively, for the second harmonic output. The phase noise is -120 dBc/Hz at offset frequency 100 kHz for the fundamental frequency. However, the noise floor of fundamental phase noise in Fig. 6 is about -130 dBc/Hz because the fundamental output power is low (about -25 dBm). Therefore, it limits the phase noise measurement when the offset frequency is greater than 100 kHz for the fundamental. On the other hand, the measured phase noise for the single DRO is -117 dBc/Hz at offset frequency 100 kHz. It can be observed that the phase noise is improved slightly from the single DRO to the push-push DRO because the phase noise may not be dominated by the coherent noise of the MMICs. The imbalance of two oscillators will degrade the phase noise and the fundamental suppression, which can be observed from the simulations. Therefore, the phase noise and the suppression of the push-push DRO can be further improved by combining two MMIC chips into single one.

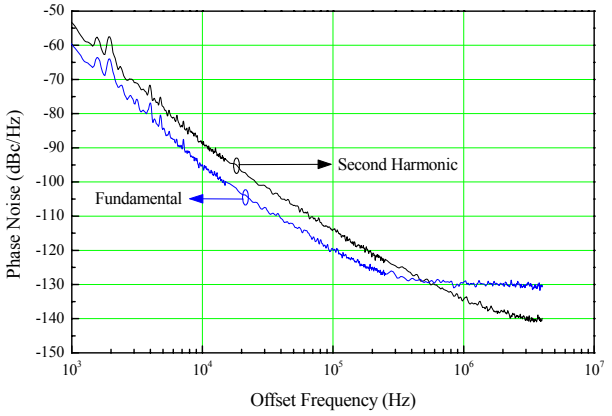

Fig. 6. Measured phase noise for the fundamental and second harmonic of push-push DRO against offset frequency from 1 kHz to 4 MHz.

IV. Conclusion

A 22-GHz ultra low phase noise push-push DRO has been implemented. By using MMIC oscillator chips, two nearly symmetric fundamental oscillators constructed. This circuit exhibits a -114-dBc/Hz phase noise at offset frequency 100-kHz, a fundamental suppression of 30 dBc and a RF output of 6 dBm. For high-level digital modulation applications, an additional phase-lock-loop (PLL) can be used together with this push-push DRO to synchronize frequency and prevent frequency drift.

Acknowledgement

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TABLE I

FOM CALCULATIONS FOR PUSH-PUSH DROS

Ref.	[5]	[6]	[7]	[8]	This Work
Features	FET Hybrid	FET Hybrid	FET Hybrid Injection-locked	Si/SiGe HBT Hybrid	2 μm GaAs HBT MMIC/Hybrid
Frequency (GHz)	34	94	22	58	22
P_{RF} (dBm)	3	0	0	-14	6
Phase Noise (dBc) @ 100 kHz	-100	N. A.	-100	N. A.	-114
Phase Noise (dBc) @ 1 MHz	N. A.	N. A.	N. A.	-112	-134
Suppression (dBc)	< -20	N. A.	N. A.	< -17	< -30
P_{DC} (mW)	480	150	N. A.	N. A.	264
FoM (dB)	183	N. A.	N. A.	N. A.	196.6
FoM (dB) Without P_{DC}	210.6	N. A.	206.9	207.3	220.8