

A Monolithic HBT Broadband Amplifier Using Modified Triple Darlington Configuration

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Abstract — A broadband Darlington amplifier has been successfully developed using commercial 2- μm GaAs HBT process. In contrast to conventional Darlington pair, a modified triple Darlington configuration is employed to achieve a bandwidth of half f_T and equalizer-type matching network is used to substitute the conventional feedback for wide bandwidth. This circuit demonstrates a measured gain of 12.8 dB from 0.3 to 19 GHz.

I. INTRODUCTION

The transmission capacities of optical communication systems and wireless applications in the millimeter-wave range have increased rapidly. Broadband amplifiers are key components of broadband communication systems, e.g., the preamplifiers in fiber-optical applications and general gain blocks in wireless systems. High gain and wide bandwidth are required for systems operating at high data rates. The high gain of Darlington pair allows circuit designers using feedback or other techniques for flat power gain over wide bandwidth.

Several architectures of Darlington pairs including two-transistor pair and three-transistor pair have been reported [13]. The most common used Darlington pair consists of an emitter-follower and a common-emitter bipolar transistors. In the earlier published Darlington amplifiers [2]-[5], the conventional Darlington pair was used as the amplifier core. However, the conventional Darlington pair suffers from the Miller multiplication of base-collector capacitance and thus resulting a narrow bandwidth. In order to resolve this problem, a common collector transistor was used to replace the emitter follower transistor [6]-[9]. In order to achieve higher gain at high frequencies, another type of Darlington pair, which is the triple Darlington configuration (or triple Darlington), was reported [14], but it still suffers from the Miller effect.

In order to achieve a flat power gain performance over wide bandwidth, some circuit design techniques are used in broadband amplifier design. Resistive feedback method is the most commonly used for flat power gain response. Another method is to use equalizer-type matching network [15]. This matching network eliminates low frequency gain and keeps the gain at high frequency for a flat gain over wide bandwidth.

In this work, a modified triple Darlington is employed as the amplifier core. Two common collector transistors are used to replace the two emitter-follower transistors to reduce the Miller effect. From the simulation results, it also demonstrates higher maximum available power gain (G_{max}) than that of other Darlington pairs. In addition, an equalizer-type matching network is also used for flat gain over wide bandwidth. This circuit demonstrates a 3-dB bandwidth with 12.8-dB gain from 0.3 to 19 GHz, which is almost half f_T .

II. DEVICE TECHNOLOGY

The MMIC process is a standard 2- μm GaAs power hetero-junction bipolar transistor (HBT) process provided by WIN Semiconductors. The HBT device used in this design has an emitter area of 1 finger \times 2 μm \times 10 μm . It has a peak f_T of 40 GHz and peak f_{max} of 100 GHz when biased at 3.5-V V_{CE} and 5-mA I_{C} . Other passive components including thin film resistor, MIM capacitors and spiral inductors are also available. The wafer is thinned to 4-mil for the gold plating of the backside and reactive ion etching via holes are used for dc grounding.

III. CIRCUIT DESIGN

Fig. 1(a) shows the triple Darlington, which is suitable for wide bandwidth (up to half f_T) design with moderate power gain [14]. However, the transistors Q1 and Q2 in triple Darlington still suffer from the Miller multiplication of its base-collector capacitance. The modified triple Darlington is shown in Fig. 1(b). The collectors of Q1 and Q2 to the output are not connected. The capacitor in the collector of Q1 and Q2 is the RF bypass capacitor to provide RF ground for the collectors of Q1 and Q2. Fig. 2 presents the G_{max} simulation results of three types of Darlington configurations. It is observed that triple Darlington improves the G_{max} only at higher frequencies and the modified triple Darlington can improve the G_{max} from dc to high frequency significantly.

The equalizer-type matching network is composed of a series inductor and a resistor shunt at the input port of triple Darlington. This matching network at the input

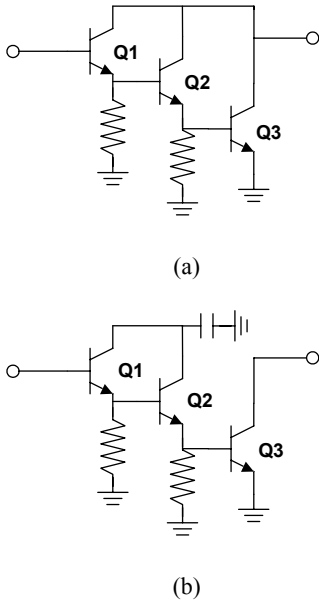


Fig. 1. The schematic diagram of the (a) triple Darlington, and (b) modified triple Darlington.

port has flat G_{\max} characteristics of the triple Darlington. As frequency increases, the inductor prevents the current flowing through the resistor while the current at the input of triple Darlington increases. As a result, the total power gain of the triple Darlington remains constant for a wide frequency range.

The complete circuit schematic diagram is shown in Fig. 3. Two triple Darlington stages are cascaded for high power gain. There are dc blocking capacitors at both input and output ports. The chip photo is shown in Fig. 4 with a chip size of $1.5 \times 1 \text{ mm}^2$.

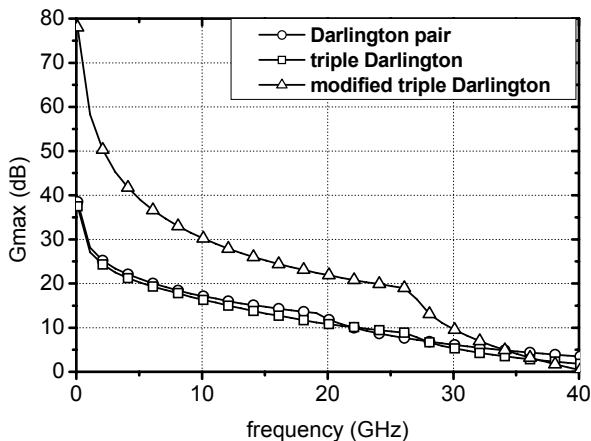


Fig. 2. Simulated G_{\max} of three different Darlington configurations.

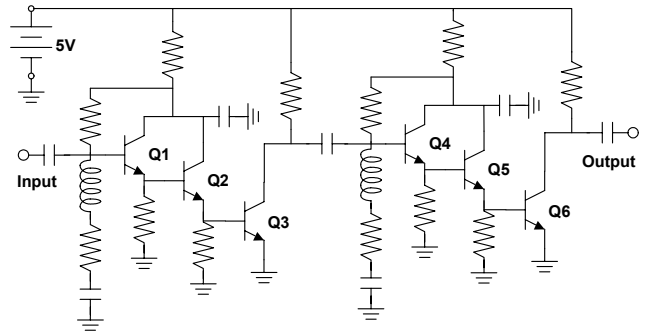


Fig. 3. Complete circuit schematic diagram of the modified triple Darlington amplifier with the equalizer-type matching network composed of a series inductor and resistor shunt at the input of the triple Darlington.

IV. EXPERIMENTAL RESULTS

The broadband Darlington amplifier was measured via on-wafer probing using Agilent 8510C vector network analyzer. Fig. 5 presents the measured gain and return losses to 30 GHz. The measured gain is 12.8 dB with 3-dB bandwidth from 0.3 to 19 GHz. The input and output return losses are better than 10 dB from 3 to 25 GHz. The group delay calculated from the measured S-parameter is shown in Fig. 6. The group delay of this circuit is $48.5 \pm 7.5 \text{ ps}$. The small variation of group delay over wide frequency range indicates low signal dispersion and thus this circuit will have a good eye opening in the eye diagram.

Fig. 7 shows the power performance of this circuit. The output power versus input power at 5 GHz, 11 GHz and 19 GHz are measured. The $P_{1\text{dB}}$ at 5, 11 and 19 GHz are 0 dBm, -4.3 dBm and -6.7 dBm respectively. In order to have higher device f_T and f_{\max} , the device size can not be too large and this limits the power performance of this circuit.

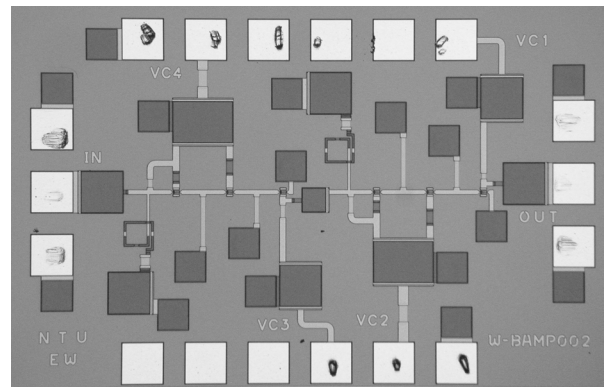


Fig. 4. The chip photo of the modified triple Darlington amplifier with a chip size of $1.5 \times 1 \text{ mm}^2$.

V. CONCLUSION

A broadband monolithic HBT amplifier has been designed, fabricated and tested. A modified triple Darlington is used to extend bandwidth. In addition, an equalizer-type matching network is also employed for flat gain over wide bandwidth of the triple Darlington instead of resistive feedback. This chip achieves 12.8-dB power gain with 3-dB bandwidth from 0.3 to 19 GHz with a chip size of $1.5 \times 1 \text{ mm}^2$.

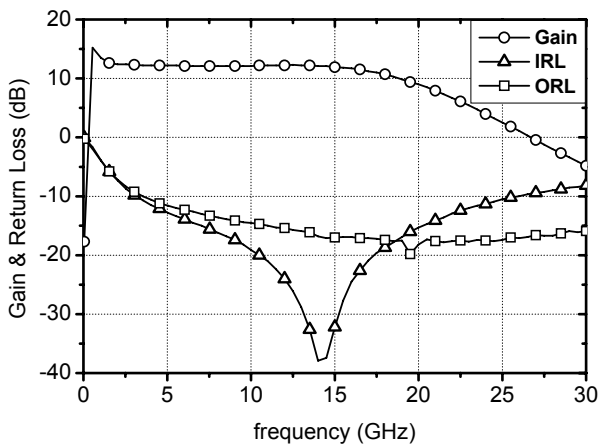


Fig. 5. The measured gain and return losses from 0.3 to 30 GHz.

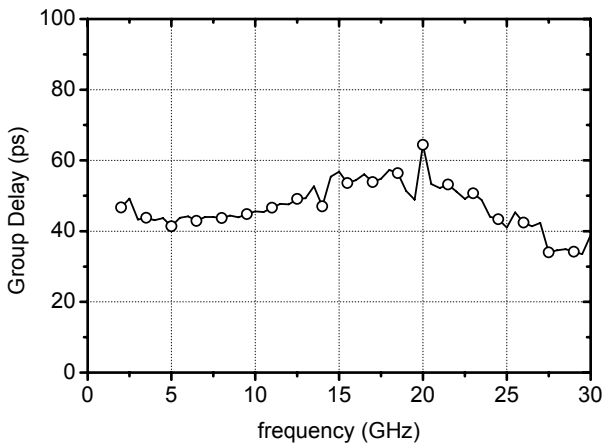


Fig. 6. The group delay calculated from measured S-parameter. The group delay is $48.5 \pm 7.5 \text{ ps}$ to 19 GHz.

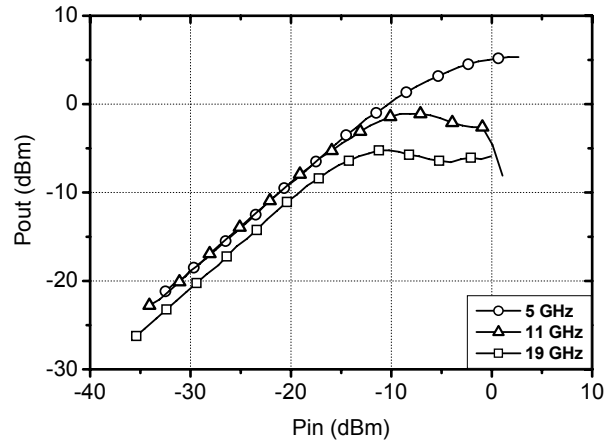


Fig. 7. The output power versus input power at 5, 11 and 19 GHz. The $P_{1\text{dB}}$ at 5, 11 and 19 GHz are 0 dBm, -4.3 dBm and -6.7 dBm respectively.

ACKNOWLEDGEMENT

The authors would like to thank Hong-Yeh Chang and Kun-You Lin on circuit testing. This work is supported in part by National Science Council (NSC 93-2752-E-002-002-PAE, NSC 93-2219-E-002-016, NSC 93-2219-E-002-024 and NSC 93-2213-E-002-033). The chip is fabricated by WIN semiconductors.

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