Submicrometer InAlAs/InGaAs Double-Gate HEMT's on Transferred Substrate

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***Abstract* — This paper reports fabrication, DC and RF characterization of the $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ double-gate HEMTs with sub-micron gate lengths. These devices present a maximum extrinsic transconductance g_m of 2650 mS/mm with a corresponding drain current I_d equal to 310 mA/mm. This extrinsic transconductance is the highest value ever reported for any transistor. Low output conductance g_d is obtained, denoting the reduction of short channel effects. The combined high transconductance and the low output conductance induce an extremely high intrinsic unloaded voltage gain (g_m/g_d) of 87.**

I. Introduction

The demand for high bit rate communication and millimeter wave applications requires the development of devices with high cut-off frequencies. One candidate for these applications is the HEMT, using InAlAs/InGaAs materials on InP substrate. At the present time, the state of the art is a cut-off frequency of 562 GHz, obtained with an InGaAs/InAlAs pseudomorphic HEMT on InP [1]. This high f_T is particularly interesting for digital circuits used in optical communication systems [2] but an improvement of the maximal oscillation frequency f_{max} is required and preferable to design analog circuits, in which a power gain is the main objective. These good results have been obtained by keeping high electron density in the side etching regions and by reducing the gate length (Lg) to 25 nm. This last condition is essential for the improvement of RF performances. Indeed, the Lg reduction allows to emphasize the velocity overshoot of the electrons in the InGaAs channel. However, the reduction of Lg alone does not lead to maximum RF performances. The so-called "short channel effects" involve a shift of the threshold voltage and a deterioration of the transconductance and the output conductance. In order to avoid these effects, the proper layer design must allow to keep a high aspect ratio Lg/a where a is the distance between the gate electrode and the two-dimensional electron gas. This scaling down rule involves a limit for HEMT's structure due to the gate tunnel current and the degradation of the effective gate length related to the depletion in the recessed regions. So, in order to increase f_T and f_{max}, it will be necessary to find alternative solutions based on a rupture of the actual technology. It can be made by using the transferred substrate technique, already used in SOI-MOSFET [3], TS-HBT [4], TS-HEMT [5]. This technique can be used for the realization of transistor with double-gate, one gate being placed on each side of the conductive InGaAs channel (figure 1). This device is particularly interesting for improving short-channel effects. Indeed, this device allows to counteract the effect of carrier injection in the buffer (no buffer is used in this structure), leading to low output conductance g_d. A good pinch-off behavior and a high transconductance are also expected due to the better charge control efficiency. Moreover, the layer structure of this device leads to a reduction of the sheet resistance and a higher two-dimensional electron gas (2DEG) density in the channel in order to obtain lower parasitic resistances.

In this way, we have realized sub-micron transferred-substrate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ double-gate HEMTs (DG-HEMT) on a 2-inch GaAs host substrate. DC and RF characteristics of these novels devices are presented.

II. Device Structure and Fabrication Process

A. Device structure

Lattice-matched InAlAs/InGaAs DG-HEMT layers are grown on a 2-inch InP substrate by gas source Molecular beam Epitaxy (Riber 32P). Figure 2 shows the cross section of the layer structure before bonding on GaAs substrate.

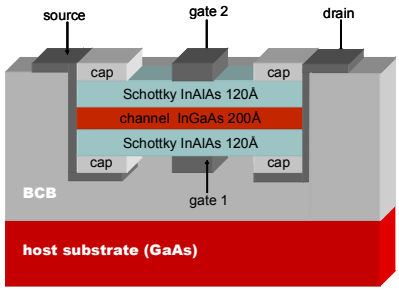

Figure 1: schematic cross section of the DG-HEMT using the transferred substrate technique.

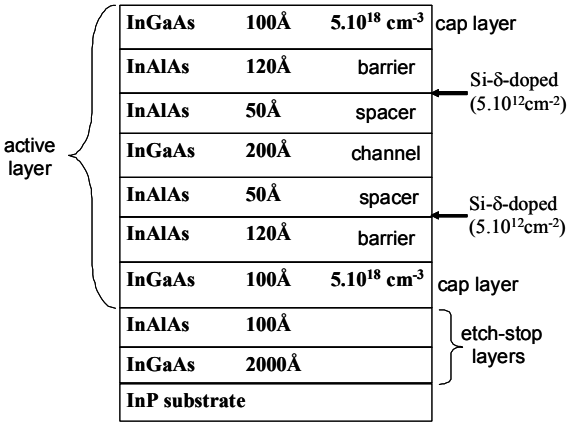

Figure 2: DG-HEMT Layer structure.

This epitaxial layer structure starts with two etch-stop layers: a 2000 Å thick InGaAs layer and a thin InAlAs layer. These layers are essential to remove the InP substrate after bonding process. Then, the achievement of the DG-HEMT active layer follows. These layers are symmetrical to the channel and correspond to two single LM-HEMT layer structures. It consists of a 100 Å n+ InGaAs cap layer, a 120 Å undoped InAlAs Schottky contact layer, a Silicon delta-doping plane of 5.10^{12} cm^{-2}, a 50 Å undoped InAlAs spacer and a 200 Å undoped InGaAs channel. Next, a second 50 Å undoped InAlAs spacer, a Silicon delta-doping plane of 5.10^{12} cm^{-2}, a 120 Å undoped InAlAs Schottky contact layer and finally a 100 Å n+ InGaAs cap layer are grown. After etching etch-stop layers, the sheet resistance is 130 Ω.

B. Fabrication Process

Figures 3.a to 3.d show the main steps of the DG-HEMT fabrication process.

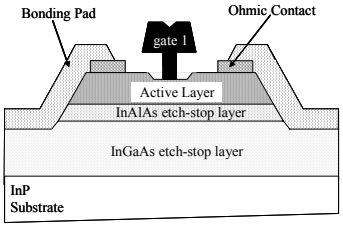

Figure 3.a: Classic HEMT realization.

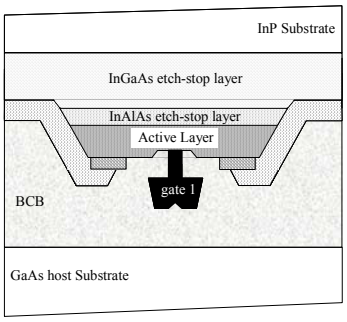

Figure 3.b: bonding on GaAs host substrate.

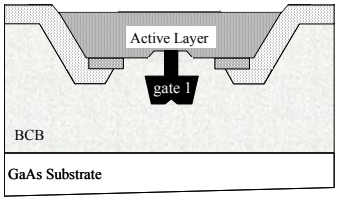

figure 3.c: etching of the InP substrate and etch-stop layers.

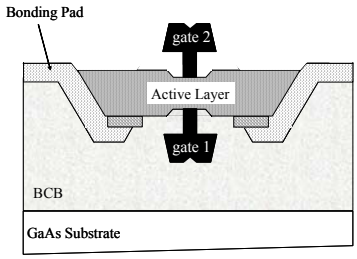

figure 3.d: second gate's realization.

The first step consists in processing a conventional HEMT (mesa, ohmic contacts, bonding pads and first gate) (figure 3.a). The device isolation is achieved by wet chemical etching using a H_3PO_4:H_2O_2:H_2O solution. Source and drain ohmic contacts are formed using Ni/Ge/Au/Ni/Au at 295 °C during 25 seconds in a nitrogen atmosphere. Typical ohmic contact resistance of about 0.09 Ω.mm is measured by transmission line method. Next, Ti/Au/Ti metallization is evaporated to form the bonding pads. In that case, the final Titanium layer allows to improve the adhesion of the bonding pads on the BenzoCycloButene polymer (BCB). The gate-recess process is carried out by wet chemical etching using a solution of Succinic Acid (SA), ammonia and hydrogen peroxide (SA:NH_4OH:H_2O_2).The first gate metallization consists of a Ti/Pt/Au/Ti evaporation.
The next step is to bond the wafer on GaAs host substrate (figure 3.b). The use of BCB has seemed to be the most appropriate polymer because it has good electrical properties: low dielectric constant (ε_R # 2,6) and low dielectric losses (tan δ # 5.10^{-4}). In addition, the bonding process is simple to implement. This process consists in depositing BCB on both the active wafer and on the GaAs host substrate and bonding it. Finally, the device has been placed into the furnace in order to cure the BCB for ensure resistance to subsequent processing operations.

After curing the BCB, the InP substrate is removed by a hydrochloric solution and the InGaAs etch stop layer is selectively etched by SA, ammonia and hydrogen peroxide. The thin InAlAs etch stop layer is etched by a H_3PO_4:H_2O_2:H_2O solution (figure 3.c). In order to control the etching, this solution is highly diluted.

Finally, the second gate-recess process is realized and the Ti/Pt/Au metallization is evaporated to form the second gate (figure 3.d).

Both gates are connected to the access pads. Figure 4 shows a SEM image of a DG-HEMT device cross-section.

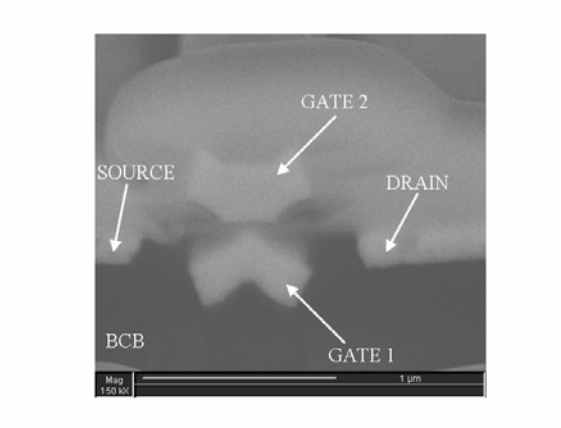

Figure 4: SEM image of the DG-HEMT.

Both gates have a different length, 100 nm for the gate 1 and 280 nm for the gate 2. However, gate 1 and gate 2 are correctly aligned.

III. Device Characterization

Output characteristics and transfer characteristics of a DG-HEMT with a width of W=2x50µm are given figure 5 and figure 6 respectively. These characteristics have been compared with a conventional HEMT with a gate length of 100nm and with the same width. This conventional HEMT has been realized with a single classic heterostructure and with the same technological process.

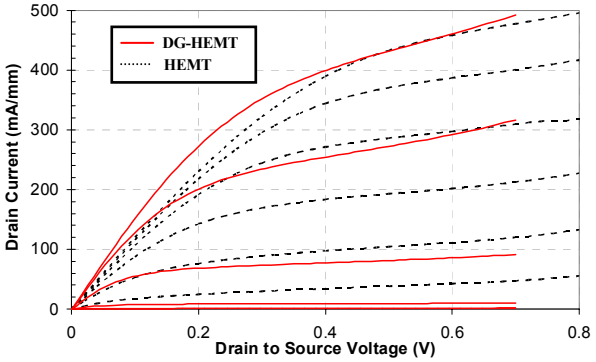

Figure 5: Output characteristics of DG-HEMT and HEMT. The gate bias for the top curves is 0.2 V and the measurement step of the gate bias is -0.1 V.

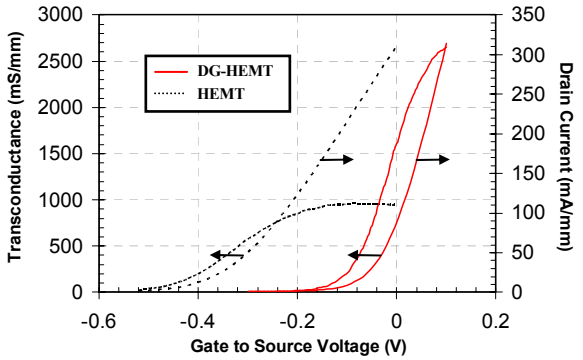

Figure 6: Transfer characteristics of DG-HEMT and HEMT at Vds=0.7V.

Threshold voltage of the DG-HEMT is -0.15 V and the maximum drain current (I_d) is 500 mA/mm. The extrinsic transconductance (g_m) reaches a maximum value of 2650 mS/mm. This value is more than two times the value of the conventional HEMT devices (960 mS/mm). However the drain current of the DG-HEMT is weak for a layer structure with two delta-doping planes. To understand these results, we performed Monte Carlo (MC) simulations for 100nm-gates lattice-matched InGaAs/InAlAs DG-HEMT and for 100nm-gate lattice-matched InGaAs/InAlAs HEMT with the same layer structure of realized devices. Figure 7 shows transfers characteristics of DG-HEMT and HEMT at V_{ds} of 1.2 V.

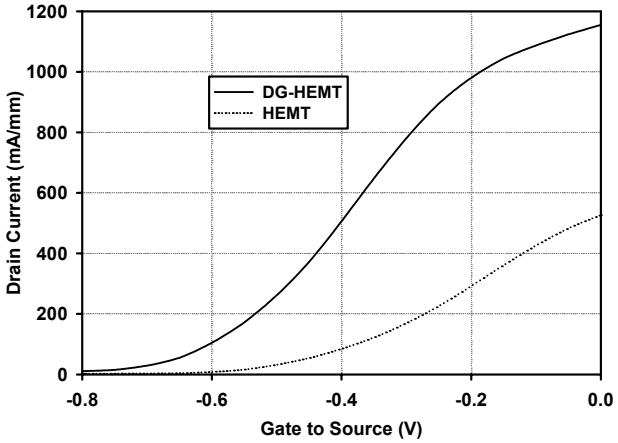

Figure 7: Transfer characteristics of DG-HEMT and HEMT at Vds=1.2V obtained by MC simulations.

We show that the drain current of DG-HEMT is two times higher than the conventional HEMT and, by differentiating the drain current with respect to V_{gs}, DG-HEMT exhibits a transconductance (2780 mS/mm) two times higher than the HEMT (1380 mS/mm). Moreover, the threshold voltage is more negative for the DG-HEMT than for the HEMT and the difference between them is $|\Delta V_{th}| = 0.2$ V. Contrary to MC simulation predictions, on the realized devices, the threshold voltage is more negative for the HEMT than for the DG-HEMT and $|\Delta V_{th}|$ is about 0.4 V.

The technological process explains these observations. Indeed, in order to etch the InGaAs etch-stop layer, we have used a SA solution which the selectivity with the InAlAs etch-stop layer was about 50. So, the 100 Å InAlAs etch-stop layer was partly etched. Moreover, this layer has been etched by using a non-selective solution (H_3PO_4). Consequently, the second cap layer has been partly etched leading to a lower 2DEG density in the channel and a lower drain current. And finally, due to a thinner cap layer, the second recess process has partly etched the barrier layer leading to a shift of the threshold voltage. Moreover, a ratio higher than 2 between transconductances of DG-HEMT and HEMT obtained with realized devices is related to the decrease in the distance between the gate electrode and the channel.

The S-parameters of the DG-HEMTs are measured on wafer from 0.5 to 50 GHz using a vector network (HP8510C). Frequency dependence of current gain

($|H_{21}|^2$) and Mason's unilateral power gain (Ug) are shown figure 8. Based on the usual 6dB/octave extrapolation, the device exhibits a f_T of 110 GHz and a f_{MAX} of 200 GHz. These low values are related to the long gate (Lg =280 nm).

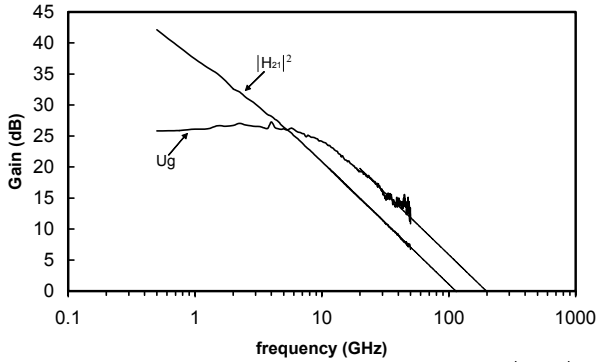

figure 8 : frequency dependence of current gain ($|H_{21}|^2$) and Mason's unilateral power gain (U_g) for DG-HEMT First gate and second gate length are 100nm and 280nm respectively.

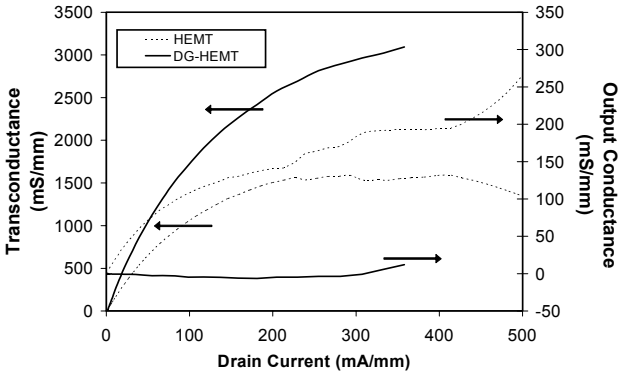

figure 9 : Intrinsic transconductance and intrinsic output conductance versus drain current for DG-HEMT and for HEMT.

On figure 9, the intrinsic transconductance g_m and the intrinsic output conductance g_d of the DG-HEMT are compared with a conventional HEMT (Lg = 100 nm, W=2x50µm).

For the DG-HEMT, the intrinsic transconductance g_m is higher than 3100 mS/mm. At the same bias voltage, the intrinsic output conductance g_d is weakened significantly. Consequently, the intrinsic unloaded voltage gain (g_m/g_d) has an extremely high value of 87.

For the conventional HEMT, this ratio is only equal to 8. For the DG-HEMT, g_d is strongly reduced, particularly near the pinch-off voltage, due to the removal of the buffer layer and the better charge control efficiency.

IV. Conclusion

In this paper, the technological realization of the first double gate InAlAs/InGaAs HEMT (DG-HEMT) with sub-micron gate lengths using a transferred substrate technique has been presented. An excellent transconductance and a lower output conductance have been obtained indicating clearly the effect of the second gate on the charge control efficiency. Moreover, the high unloaded voltage gain (g_m/g_d) presents a huge value, particularly near the pinch-off voltage, indicating the reduction of short channel effects.

Acknowledgement

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