Analytical Expressions for Distortion of SOI MOSFETs using the Volterra Series

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***Abstract*— The harmonic and intermodulation distortions of SOI MOSFETs are studied with the help of the Wiener-Volterra series. Simple relationships are given and validated through Large-Signal Network Analyser measurements. The simplicity of the formulation makes it attractive to circuit designers. Furthermore, it may be used to determine the validity range of low-frequency based distortion characterization techniques. It is shown that the dominant poles of the HD for a 0.25 μm Partially Depleted SOI MOSFET lies at a few GHz, depending on the load impedance and the biasing and that its IMD_3 depends on the tone separation.**

I. Introduction

Silicon-on-Insulator (SOI) is one of the most promising low cost technology for integrated low-voltage, low-power circuits operating at microwaves [1]. The distortion characterization of SOI nMOSFET is investigated in function of the frequency in this paper. Nevertheless, the models derived are compatible with other FET technologies.

The interest for nonlinear analysis has grown recently, as distortion is responsible for the generation of spurious frequency bands in telecommunication circuits. The origin of nonlinearities are explained by the semiconductor physics. The DC drain current exhibits a highly nonlinear characteristic when the drain and gate voltages (V_G and V_D, resp.) are varied. At high frequency of operation, the effect of reactances is no more negligible. Nevertheless, previous experimental work showed that the distortion is dominated by the current-voltage ($I-V$) characteristic up to radio frequencies (RF) [2].

So most available distortion characterization techniques are based on drain current DC measurements. Indeed, a Taylor series analysis gives the distortion through the calculation of high-order derivatives of the $I-V$ characteristics and it has been widely used to analytically model the weak nonlinear behavior of transistors [3]. This method is unfortunately not suitable for high-frequency (HF) analysis. More recently, an integral function method (IFM) [4], [5] was proposed with the advantage to be less sensitive to the measurement noise.

The analytical frequency dependent representation of a system with memory effects requires the use of the Volterra series [6], [7]. If all nonlinear elements are modeled, this technique leads to huge expressions that may only be evaluated by computers [8], [9]. However, circuit designers need *simple expressions* that describe the large signal behavior of the transistor in function of the main design parameters. Specific piece of equipment is required to get the large-signal behavior of a device or a circuit at HF. For instance, a Large-Signal Network Analyzer (LSNA) provides both phase and amplitude of the signal and its harmonics up to a few GHz [10]. It was used to validate the present analysis.

The purpose of this work is to provide simple methods to characterize and predict harmonic and intermodulation distortion (HD and IMD, resp.) of a MOSFET that are valid at low frequency (LF) as well as at HF. The formulation has two main advantages over the previous ones. First, due to its simplicity, it is helpful to the circuit designer that wants to determine the evolution of HD in function of the load impedance and the frequency. Second, it will be used to set the frequency validity range of the characterization techniques based on DC measurements.

II. Distortion analysis of a MOSFET from an equivalent circuit

As already mentioned, the main nonlinearities in a MOSFET arise from the drain current shape. Not only the transconductance but also the output conductance affect the nonlinear behavior of the device [11], [5]. In this section, we analyze the case where the nonlinearity can be described accurately by a third order Taylor series expansion. In this case, the drain current I_D may be assumed to be equal to:

$$I_D = I_{D0}+g_{m1}V_G+g_{m2}V_G^2+g_{m3}V_G^3+g_{d1}V_D+g_{d2}V_D^2+g_{d3}V_D^3 \quad (1)$$

where g_{mi} (g_{di}) are proportional to the i^{th} derivative of $I_D(V_G)$ ($I_D(V_D)$). Note that the cross-derivatives are not taken into account. As discussed in [11], this model is well appropriated to analyze the distortion of a MOSFET in the saturation region. In the linear region however, the cross-modulation terms should be added.

The main limitation of the analysis provided here is that the nonlinear elements have to be described in term of the Taylor-series expansions of their characteristic. The derivatives of the characteristic at any bias point must so remain constant over the AC voltage and current deviation from the bias point. To ensure the valid representation of the Taylor series, the nonlinearity should be weak enough and the excitation signals small enough.

In CMOS technologies the capacitive elements do not generate any significant harmonics but they should be included to get the proper behavior of the transistor [11]. Indeed, C_{gd} acts as feedback loop and high-frequency signals are shunted through capacitors.

The Volterra kernels are calculated by the method of nonlinear currents applied to the simple equivalent circuit of a MOSFET presented in Fig. 1. The large-signal figures of merit are evaluated from that kernels and the expressions are later approximated as follows:

$$HD_2(f) \approx HD_{2DC}\frac{1+jf/f_{zHD_2}}{1+jf/f_{pHD_2}} \quad (2)$$

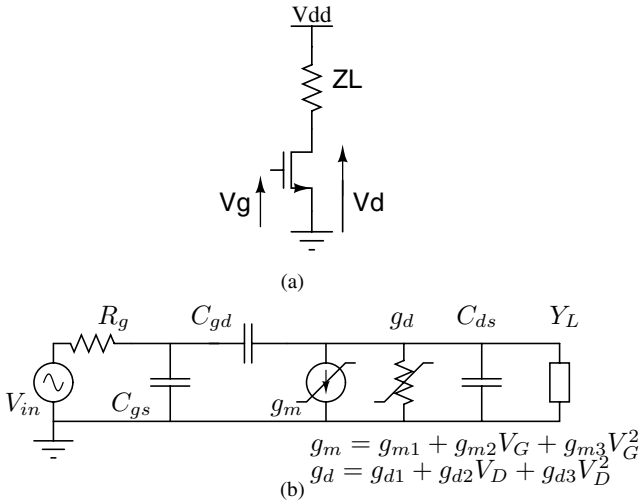

Fig. 1. Common-source MOSFET configuration (a) and its equivalent schematic (b) used in the Volterra series analysis.

with

$$HD_{2DC} = \frac{V_{in}}{2}\left|\frac{g_{m2}}{g_{m1}} + \frac{g_{d2}g_{m1}}{Y_L^{'2}}\right| \quad (3)$$

$$f_{zHD_2} = \frac{1}{4\pi}\left[R_g(C_{gd}+C_{gs}) + \frac{g_{m2}Y_L^{'}(C_{ds}+C_{gd}) - g_{d2}g_{m1}C_{gd}}{g_{m2}Y_L^{'2} + g_{d2}g_{m1}^2}\right]^{-1} \quad (4)$$

$$f_{pHD_2} = \frac{1}{2\pi}\left[3R_g\left(C_{gd}\left(\frac{g_{m1}}{Y_L^{'}}+1\right)+C_{gs}\right) + 3\frac{C_{ds}+C_{gd}}{Y_L^{'}} - \frac{C_{gd}}{g_{m1}}\right]^{-1} \quad (5)$$

$$Y_L^{'} = g_{d1} + \frac{1}{Z_L} \quad (6)$$

and

$$HD_3(f) \approx HD_{3DC}\frac{(1+jf/f_{z1HD_3})(1+jf/f_{z2HD_3})}{(1+jf/f_{p1HD_3})(1+jf/f_{p2HD_3})} \quad (7)$$

with

$$HD_{3DC} = \frac{V_{in}^2}{4}\left|\frac{(-g_{d3}Y_L^{'}+2g_{d2}^2)g_{m1}^2}{Y_L^{'4}} + \frac{2g_{d2}g_{m2}}{Y_L^{'2}} + \frac{g_{m3}}{g_{m1}}\right| \quad (8)$$

$$f_{z1HD_3} = \frac{2g_{d2}^2 - Y_L^{'}g_{d3}}{4\pi\left[(ag_{d3}-2R_g g_{d2}^2)C_{gd} + g_{d3}C_{ds} + (-2R_g g_{d2}^2 + g_{d3}Y_L^{'}R_g)C_{gs}\right]} \quad (9)$$

$$f_{z2HD_3} = \frac{1}{6\pi R_g C_{gd}} \quad (10)$$

$$f_{p1HD_3} = \frac{-Y_L^{'}/2\pi}{\left[7C_{gd}\left(a - \frac{Y_L^{'}}{7g_{m1}}\right) + 4(C_{ds}+Y_L^{'}R_g C_{gs})\right]} \quad (11)$$

$$a = 1 + R_g(g_{m1} + Y_L^{'}) \quad (12)$$

$$f_{p2HD_3} = \frac{-g_{m1}}{2\pi C_{gd}} \quad (13)$$

Note that (3) and (8) are the factors given by a Taylor analysis.

Following the same methodology, two-tone analysis may be performed. In order to simplify the expressions, C_{gd} was neglected. It was also assumed that the the tones are close together with regard to the operation frequency ω and that the global output conductance $G_o(\omega) = Y_L + g_{d1} + j\omega C_{ds}$ verifies $G_o^*(\omega) = G_o(-\omega)$. Then, the intermodulation distortion of order 3 (IMD_3) is given by:

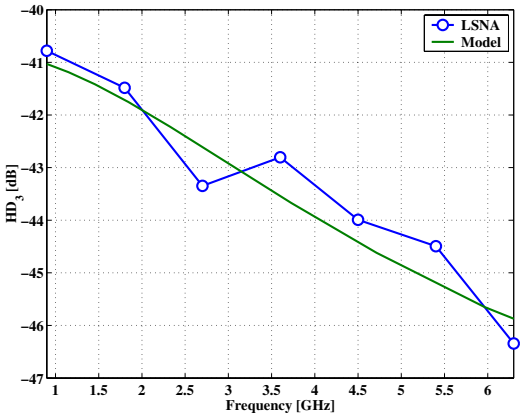

Fig. 2. HD_3 from 900 MHz LSNA measurements and our model; $V_D = V_G = 1.2$ V; applied AC magnitude is $V_{in} = 0.3$ V.

$$IMD_3 = \frac{3}{4}V_{in}^2\frac{1}{1+\omega^2 R_g^2 C_{gs}^2}|IM_3| \quad (14)$$

where

$$IM_3 = \frac{g_{m3}}{g_{m1}} - \left(\frac{g_{m1}}{G_o(\omega)}\right)^2\frac{g_{d3}}{G_o^*(\omega)} + \frac{2}{3}g_{d2}g_{m2}\left(\frac{1}{G_o(2\omega)G_o^*(\omega)} + \frac{2}{G_o^*(\Delta\omega)G_o(\omega)}\right) + \frac{2}{3}\left(\frac{g_{m1}}{G_o(\omega)}\right)^2\frac{g_{d2}^2}{G_o^*(\omega)}\left(\frac{1}{G_o(2\omega)} + \frac{2}{G_o^*(\Delta\omega)}\right) \quad (15)$$

It follows from (14) that the IMD_3 not only depends on the third-order nonlinearity of the transconductance as commonly assumed, but also on the output conductance at low-frequency and at the second harmonic. As G_o of a Partially-Depleted (PD) SOI MOSFET is frequency dependent, we expect from relation (14) to measure a variation of IMD_3 in function of the tones separation for that device [12]. This will be discussed in the next section.

III. Experimental results

The Device under Test (DuT) that is considered through this analysis, is a PD SOI nMOS composed of 12 fingers connected in parallel, 6.6 μm width and 0.25 μm length each, built at CEA-LETI, France, following a 0.25 μm process. The extracted threshold voltage V_{th} is 0.56 V. All measurements were performed on-wafer with the source of the MOSFET grounded.

The accuracy of the expressions given in the previous section were checked by comparing them to LSNA measurements. As shown in Fig. 2, the frequency behavior is well represented by the model.

It appears from the previous section that the HF behavior of HD may be characterized by poles and zeros. Their value depends on the bias point of the MOSFET and on the load impedance. For our DuT and for most bias points, the zeros of (2) and (7) lie at higher frequency than their poles. Furthermore, in (7) the dominant pole and zero are respectively f_{p1HD_3} and f_{z1HD_3}. In other words, both HD_2 and HD_3 are almost constant until the frequency f_{pHD_2} or f_{p1HD_3} is respectively reached. It may be seen in Fig. 3 that the HD

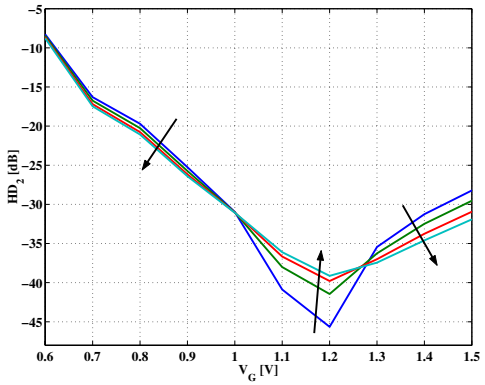

Fig. 3. HD_2 evaluated by (2) for frequencies between 1 MHz and 12 GHz. The arrows indicate a frequency increase. $V_D = 1.2$ V, $V_{in} = 0.3$ V; $Z_L = 50\ \Omega$.

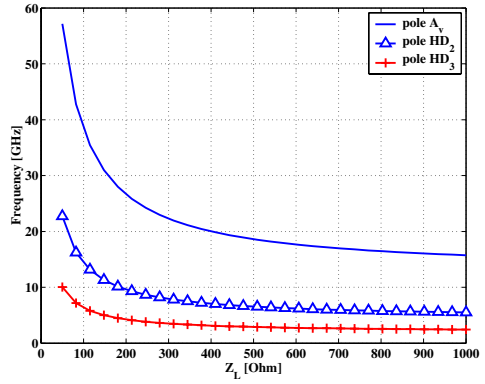

Fig. 4. Poles of HD and voltage gain of our DuT; $V_D = V_G = 1.2$ V.

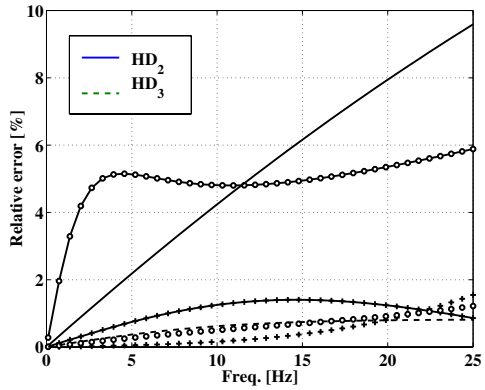

Fig. 5. Relative error between model A and model B; $V_D = 1.2$ V and $A = 0.2$ V. Dashed lines refers to HD_3 and continuous lines to HD_2. Symbols refer to different gate voltages: $V_G = 1.4$ V no symbol, $V_G = 1.2$ V circles, $V_G = 1.0$ V crosses.

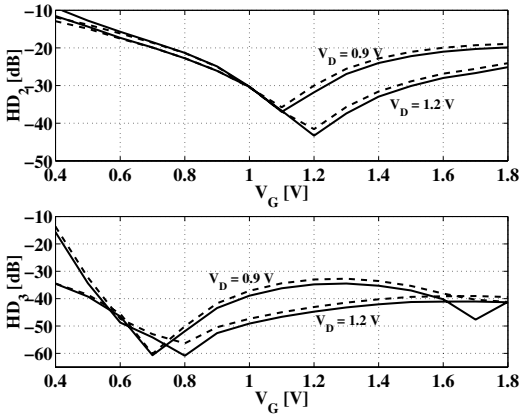

Fig. 6. Proposed analytical expressions compared to model B; frequency = 10 GHz; $V_D = 1.2$ V; $A = 0.2$ V.

predicted by the model decreases at high gate voltage with the frequency. The linear capacitances included in the model reduce the output impedance at HF. The voltage swing also decreases, increasing the effective output conductance linearity. On the other hand, only HD_2 increases with frequency at the V_G corresponding to its minimum (Fig. 3). The dominant poles are plotted in Fig. 4 in function of the load impedance Z_L. For instance, the f_{pHD2} and f_{pHD3} of our DuT loaded by $Z_L = 200\ \Omega$ are found to be about 10 GHz and 4.5 GHz, respectively. It is interesting to note that the ratio between the pole of the voltage gain A_v and the one of HD_2 (HD_3) is almost constant at relatively high value of Z_L. Furthermore, it can be concluded from relations (5) and (11) that

$$|f_{pHD_2}| \geq \frac{|f_{pA_v}|}{3} \tag{16}$$

$$|f_{p1HD_3}| \geq \frac{|f_{pA_v}|}{7} \tag{17}$$

Those last relations give us a rule of thumb to find the frequency at which the low-frequency analysis (Taylor approach or IFM, e.g.) is not valid anymore.

In order to check the assumptions of the model presented in Section II, the Kernels of Volterra were also calculated numerically with an extended version of the model, denoted *model* B. In model B, the LF drain current is again modeled as (1), but this time the three capacitances (C_{gs}, C_{gd} and C_{ds}) are also described by a third-order Taylor series. As we deal with numerical simulations, no simplifications of the kernels were done. In the following, *model* A will refer to the schematic presented in Fig. 1, i.e. the capacitances are assumed to be linear. The analytical formulation (2)-(15) is a simplified version of model A that relies on the same schematic. The importance of nonlinear capacitances is shown in Fig. 5 were the relative error between model A and model B is given for different bias conditions. Very good agreement is obtained for HD_3 (and IMD_3, as it uses the same kernels) and for HD_2 when the bias is below the minimum in Fig. 3. The analytical formulation presented in Section II was also compared to model B in Fig. 6. The relative error of the formulation increases with the frequency. We calculate that it stay below 3% (4%) at 2 GHz for HD_2 (HD_3) and below 20% at 10 GHz for both HD_2 and HD_3.

Numerical simulations permitted to analyze the relative impact of the different elements present in the equivalent circuit in Fig. 1 to the nonlinear factors of merit. At low frequency, the importance of both g_m and g_d has already been discussed previously [5]. If the drain current representation of (1) is adopted, we showed above that a good approximation of the frequency behavior may be obtained if only the linear capacitances are taken into account. However, if they are not included in the model, a 30% error relative to the complete model is obtained around 15 GHz for HD_2 and around 9 GHz for HD_3. The gate capacitance C_{gs} acts as a lowpass filter that

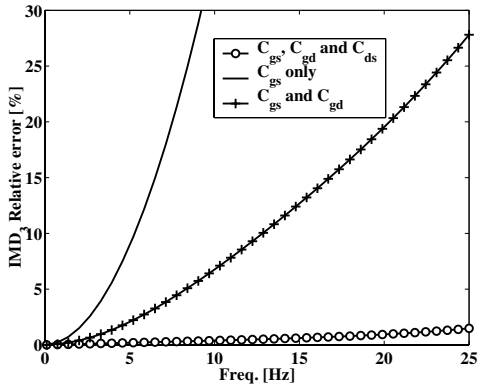

Fig. 7. Relative error to model B due to the model simplifications;$V_G = 1.0$ V; $V_D = 1.2$ V; $A = 0.2$ V.

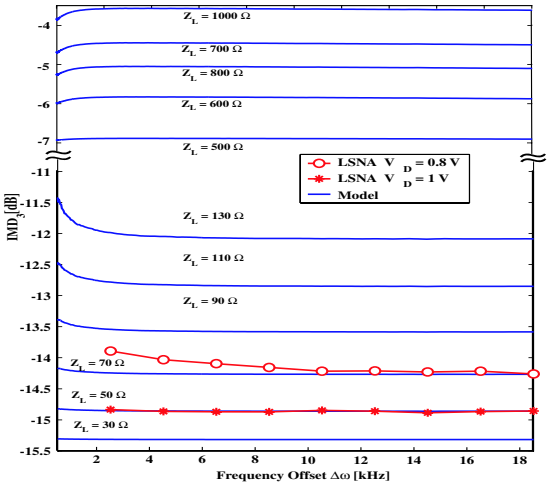

Fig. 8. IMD_3 *vs* tone separation; LSNA measurements were performed on a 50 Ω set-up. $V_G = 1$ V, $V_{in} = 0.6$ V.

decreases the amplitude of the input signal. Thus, a high value of C_{gs} leads to a lower distortion level but, as the distortion is the ratio between output and input signals, it is not much affected by C_{gs}. Simulations showed that C_{ds} also has a minor impact on the distortion factors of merit, as it does not change much with the bias. Furthermore, it contributes to lower the distortion level, as it filters the output admittance. Only C_{gd} has a strong influence on the HD because it models the feedback of the transistor. Numerical results in Fig. 7 confirme this discussion for linear capacitances. The relative error to model B is plotted in three when only C_{gs} is present, when C_{gs} and C_{gd} are presents, and when the three capacitances are taken into account.

The model highly relies on the extraction of the small-signal elements in Fig. 1. The procedure presented in [13] was used for that purpose. A sensitivity analysis was performed to see the impact of a wrong evaluation of the elements of the equivalent circuit. Numerical simulations showed that if these elements vary within 10% of their nominal value, the relative error is in any case inferior to 20%. The error is dominated by the drain current model of (1). Typically, depending on the bias conditions, a maximum value of 10% error on HD_3 at 5 GHz is evaluated for a 10% variation of g_{di} and g_{mi}, g_{m1} and g_{d3} having the highest impact. The formulation is almost independent of a variation of C_{gs} and C_{ds}, i.e. the error is smaller than 1%. However, the error due to C_{gd} is more important ($< 5\%$) as it is situated in the feedback loop.

Two-tones tests were also performed by LSNA and compared to simulations obtained by the Volterra-based model. It appears that, for bias points where the $I - V$ exhibits a kink ($V_D = 0.8$ V for our DuT), as the output conductance of a PD device varies with (low) frequency, the $G_o(\Delta\omega)$ changes and IMD_3 depends on the tone separation (Fig. 8). It comes from Fig. 8 that, even if the model describes this only qualitatively, the phenomenon is more important when the impedance load is higher.

IV. Conclusions

Simple relationships based on the Volterra series analysis are given and validated through measurements and numerical simulations using a more complete model. They were used to determined the validity range of low-frequency based distortion characterization techniques. We discussed the evolution of HD in function of biasing and load impedance. As the kink effect of the PD SOI MOSFET is frequency dependent, it was shown that the IMD_3 of this device varies with the tone separation $\Delta\omega$.

Acknowledgments

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