Direct Observation of Gain Compression Mechanisms in PHEMT by RF Gate and Drain Currents

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Average rf gate and drain currents can be used to determine gain compression mechanisms for PHEMTs with different pinch-off voltages. Knee voltage, pinch-off voltage, breakdown voltage and Imax clip output I-V waveform of a PHEMT and cause gain compression. We found that there is a distinct signature in average rf gate and drain currents to characterize each gain compression mechanism in PHEMTs. A PHEMT with low pinch-off voltage behaves the same in rf gate and drain currents as a PHEMT with high pinch-off voltage in pinch-off voltage, knee voltage and breakdown voltage gain compression mechanisms, but behaves differently in Imax gain compression mechanisms.

INTRODUCTION

Knee voltage, pinch-off voltage, breakdown voltage and Imax clip output I-V waveform of a PHEMT and cause gain compression and power saturation. Meng et al have successfully used rf gate and drain currents near P_{1dB} to determine gain compression mechanisms in MESFET [1]. same approach is used The to characterize AlGaAs/InGaAs/GaAs PHEMTs gain compression mechanism in this paper. A PHEMT device differs from a MESFET device in the transconductance characteristics. In the case of a MESFET device, transconductance becomes higher when gate voltage is biased more positively. On the other hand, a PHEMT device has a maximum transconductance at a certain gate voltage because a parasitic low mobility AlGaAs MESFET starts to conduct and degrades transconductance when the gate voltage is biased beyond the maximum transcondutance region. Thus, gain compression mechanisms of two types of AlGaAs/InGaAs/GaAs PHEMTs with different pinchoff voltages are studied in this work.

DEVICE STRUCTURE AND DC CHARACTERISTICS

The two kinds of AlGaAs/InGaAs/GaAs PHEMT devices are from the same epi-wafer and were intentionally etched differently to obtain different Idss while the rest of process parameters were kept identical. Gate length is 0.35 μ m. The high current PHEMT device has 2.5 V pinch-off voltage and maximum transconductance occurs at V_{gs}=-1.5 V while the low current PHEMT device has 1.5 V pinch-off voltage and maximum transconductance occurs at V_{gs}=-0.3V. A low pinch-off voltage PHEMT device has higher gate-to-

drain breakdown voltage and thus becomes harder to observe the breakdown gain compression mechanism. I-V curves of the PHEMT device with high pinch-off voltage (150 μ m gate width) and the PHEMT device with low pinch-off voltage (250 μ m gate width) are illustrated in figure 1 and figure 2, respectively.

MAXIMUM SATURATED POWER LOAD PULL EXPERIMENTAL RESULTS

The input tuner impedance is set to maximize small signal gain while the output tuner impedance is set to maximize output power at a strong enough input power under load-pull condition. A commercial ATN load pull system is used here to acquire experimental data and all the measurements were performed at 1.8 GHz in this section. Large signal performances as a function of input power are then measured at each bias point. The exact loadline impedance does not affect gain compression mechanism when a device is biased very close to the gain compression region. Four bias points near only one gain compression region were selected for the PHEMT device with high pinch-off voltage. Figure 3 illustrates power performance, the average rf gate and drain current as a function of input power when V_{ds}=2V V_{gs}=-1.5 V (near knee voltage). The average rf gate current is zero and average drain and average drain current becomes smaller when gain compression (near P_{1dB}) occurs. The gate current is still zero even at higher gain compression point. In other words, gate is not forward-biased when knee voltage clips output waveform. The power performance and average rf currents when biased at $V_{ds}=3V V_{gs}=-$ 2.5V (near pinch-off voltage) are illustrated in figure 4. The operation changes from class A to class AB as input signal becomes larger. Thus, the average drain current increases near P1dB. However, gate current is zero

because gate is still in reverse bias when gain compression occurs. Breakdown voltage can also cause gain compression and is illustrated in figure 5 for the case of V_{ds}=5V V_{gs}=-2.5V (near breakdown voltage). Strictly speaking, figure 5 corresponds to a mixed gain compression mechanism because the device experiences pinch-off voltage gain compression slightly before the breakdown voltage gain compression mechanism. The average rf gate current becomes negative and the average rf drain current increases near P_{1dB}. The increase in drain current comes from the generation of positive drain current by avalanche at large drain voltage swing. Also, there exists negative gate current flowing into the gate when the large drain voltage swing reaches breakdown voltage. Figure 6 illustrates power performance and the average rf current when V_{ds}=4V V_{gs}=-1.5V (near Imax). The average rf gate current is zero and average drain current decreases when gain compression (near P_{1dB}) occurs because the maximum transconductance occurs at Vg=-1.5 V. A low Vp PHEMT device behaves differently in Imax gain compression mechanism as illustrated in figure 7. The drain current decreases and gate current starts to increase near P_{1dB} in figure 7. Figure 8 and figure 9 illustrate the knee voltage and pinch-off voltage gain compression mechanisms for a low Vp PHEMT device. As it can be observed in figure 4, 6, 7 and 9, the gate current at P_{1dB} is closer to the positive gate current region in the case of a low pinch-off PHEMT device because maximum transconductance voltage occurs more toward forward gate conducting voltage.

RHI AND RLO LOAD PULL EXPERIMENTAL RESULT

A device at one given bias point may have different gain compression mechanisms for various loadline impedances. The observation of R_{HI} and R_{LO} loadlines under load-pull condition using average rf gate and drain current at 1 dB gain compression point was successfully applied to MESFET [2] [3]. The same approach is also applied here to observed the loadlines for the PHEMT device with high pinch-off voltage. The selected bias point is $V_{ds}=2$ V and $V_{gs}=-1$ V. Device size is 250 μ m and measurement frequency is 2.4 GHz. Figure 10 illustrates the constant Pout load pull contour when Pin=5dBm. The power performance for R_{HI} loadline is illustrated in figure 11 and apparently the corresponding gain compression mechanism is the knee voltage. Figure 12 illustrates the power performance for maximum power loadline Ropt. The corresponding gain compression mechanism is still the knee voltage. However, the decrease in drain current is smaller because load impedance is smaller. Finally, the power performance of RLO loadline is illustrated in figure 13. The rf gate and drain current behave very differently. strong nonlinearity in transconductance The is responsible for the rf gate and drain current behavior.

CONCLUSION

In summary, all the gain compression mechanisms and their associate signatures for PHEMT devices have been discussed. A low Vp PHEMT device behaves the same in rf gate and drain currents as a high Vp PHEMT device in pinch-off voltage, knee voltage and breakdown voltage gain compression mechanisms, but differs in Imax gain compression mechanisms. Average rf gate and drain currents can be used distinguish different gain compression mechanisms such as knee voltage, pinch-off voltage, breakdown voltage and Imax in PHEMT devices.

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REFERENCES

[1] C. C. Meng, J. W. Chen, C. H. Chang, L. P.Chen, H. Y. Lee and J. F. Kuan, "Using average RF gate and drain currents to determine gain compression mechanisms for narrow-recessed and wide-recessed MESFETs," *European Gallium Arsenide and other semiconductors application symposium (GAAS* 2000), p338-341, Oct 2000.

[2] C. C. Meng, C. H. Chang, J. F. Kuan and G. W. Huang, "Direct Observation of Loadlines in MESFET by Using Average RF Gate and Drain Currents", 2002 IEEE international microwave symposium MTT-S, pp.2161-2164

[3] S.C. Cripps, *RF power amplifiers for wireless communications*, Boston, London: Artech House, 1999.



Fig. 1 I-V curves for a high Vp PHEMT device. Pinch-off voltage is 2.5 V.



Fig. 2 I-V curves for a low Vp PHEMT device. Pinch-off voltage is 1.5 V.



Fig. 3 Gain, Ig and Id vs. Pin for a high Vp PHEMT device when biased near knee voltage. Ig=0 and Id decreases near P_{1dB} .The gate current is still zero at even higher gain compression point.



Fig.4 Gain, Ig and Id vs. Pin for a high Vp PHEMT device when biased near pinch-off voltage. Ig=0 and Id increases near P_{1dB} .



Fig. 5 Gain, Ig and Id vs. Pin (dB) vs. Pin for a high Vp PHEMT device when biased near breakdown voltage. Ig<0 and Id increases near P_{1dB} .



Fig. 6 Gain, Ig and Id vs. Pin for a high Vp PHEMT device when biased near Imax. Ig=0 and Id decreases near $P_{\rm 1dB}$



Fig. 7 Gain, Ig and Id vs. Pin for a low Vp PHEMT device when biased near Imax. Id decreases and Ig increases near P_{1dB} .



Fig. 8 Gain, Ig and Id vs. Pin for a low Vp PHEMT device when biased near knee voltage. Id decreases and Ig=0 near P_{1dB} .



Fig. 9 Gain, Ig and Id vs. Pin for a low Vp PHEMT device when biased near pinch-off voltage. Ig =0 and Id increases near P_{1dB} .



Fig. 10 Constant power load-pull contour for a PHEMT device with high pinch-off voltage. $V_{ds}=2V$, $V_{gs}=-1V$ and measurement frequency is 2.4GHz.



Fig. 11 Gain, Ig and Id vs. Pin for a high Vp PHEMT device when biased at $V_{ds}=2V$, $V_{gs}=-1V$ with R_{HI} loadline. Id decreases and Ig=0 near P_{1dB} .



Fig. 12 Gain, Ig and Id vs. Pin for a high Vp PHEMT device when biased at $V_{ds}=2V$, $V_{gs}=-1V$ with Ropt loadline. Id decreases and Ig=0 near P_{1dB} .



Fig. 13 Gain, Ig and Id vs. Pin for a high Vp PHEMT device when biased at $V_{ds}=2V$, $V_{gs}=-1V$ with R_{LO} loadline.