Low-Cost Wide-Range Low-Current Consumption Linear HBT MMIC Power Amplifier for Portable 2.4GHz WLAN Applications

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***Abstract* — A low-cost, low-current consumption 2.4-2.5GHz MMIC power amplifier operating at 3.3V single supply has been developed for high data rate, wide-range portable WLAN applications. The MMIC utilizes a Fairchild-proprietary InGaP HBT process that enables the design of high power density and extremely linear circuits at frequencies exceeding 6GHz. The MMIC design has been constructed based on accurate HBT and passives models, focusing on performance optimization for low AM-AM and AM-PM distortion, low current consumption and minimal harmonic levels. For an OFDM modulated signal at 54Mbps data rate, the PA delivers +23.6 dBm linear output at a corresponding Error Vector Magnitude (EVM) of 4.4%(-27dB), while consuming an average packet current of less that 315mA. The MMIC is fully matched in a cost-effective 3x3mm QFN package, requiring only a small number of external passive components for efficient board layout and low total cost.**

I. Introduction

In recent years, the development of WLAN systems has received increased attention [1]-[2], with rapidly-growing volumes of portable wireless Network Interface Cards (NICs) and access points on the consumer market. Along with the development of more complex wireless ICs, the design of highly linear power amplifiers has been equally emphasized [3]-[5] to extend transmission range and lower system bit error rates. Today, with fully-integrated WLAN Front-End-Modules (FEMs) entering the market, system designers still rely on a wide variety of fully-discrete or partially-integrated approaches to implementing critical functions in the radio front-end. The RF power amplifier is certainly one of these key elements. Fully discrete RF front-end solutions, although requiring greater board space, are often less risky and give the end user the opportunity to choose among several suppliers achieving both the best performance and lower cost. In contrast, partial integration of multiple front-end components or critical RF tuning, such as in the case of a matched PA, may shorten system design time, provide faster time-to-market and ultimately result in more cost-effective devices. In this paper we present a 2.4-2.5GHz, cost effective, fully-matched MMIC power amplifier in a 3x3mm QFN package suitable for wider range 802.11b/g WLAN applications. For the first time, a linear output power of +23.6dBm at 4.4% EVM is reported under OFDM modulation at 54Mbps data rate at 3.3V supply voltage at corresponding linear PAE of 22% for w fully matched MMIC in a 3x3mm QFN package. The power amplifier requires only 7 total external components used for RF choking and by-passing and the integrated power detector termination.

II. MMIC Modeling and Design Details

The MMIC design was based on Fairchild's scalable, thermo-electrical HBT model [6] and extensive modeling or electromagnetic (EM) simulation of on-chip/off-chip passive circuitry and package/interconnect parasitics. The HBT model was optimized to fit small-signal data to 30GHz at collector current densities up to 20kA/cm^2 for large HBTs (>1000 um^2) and up to 50kA/cm^2 for smaller HBTs (<600 um^2). With the 23.6dBm of linear, modulated signal power, the amplifier's single-tone saturated power capability can be expected to be nearly 1W due to high peak-to-average ratio of the input signal. To achieve 25dB of gain, a 2-stage amplifier topology was selected. Quiescent current was chosen to yield a driver stage current density of <3kA/cm^2 and a current density of <1.5kA/cm^2 for the output stage at V_{CC}=3.3V. High-pass non-resonant input and inter-stage matching circuits and a low-pass resonant output matching circuit were implemented. In order to reduce losses in the matching networks, high-Q 1mil bond wires were used instead of on-chip spiral inductors. The power amplifier schematic is shown in Fig. 1. Additional features of the power amplifier include a temperature-compensated, low-reference-current enhanced bias circuit with an on-chip power shut-down control (this feature is not depicted in Fig. 1) and a temperature-compensated, DC-biased power detector that provides WLAN system designers with direct access to high dynamic range (over 20dB), peak power detection. Temperature compensation in the bias circuit is achieved by optimizing select resistors, with the primary emphasis of reducing the current roll-off at low temperatures that may have a detrimental effect on PA linearity. The bias network for the power detector serves as a temperature compensator for the detector output voltage.

It is rather intuitive to expect that AM-PM distortion can heavily affect linearity or EVM performance under OFDM modulation. Indeed, the QAM64 constellation diagram of the OFDM signal represents a set of closely spaced symbols on a Cartesian chart and even small

errors in the phase of the output signal can produce vector rotation sufficient to cause a symbol error. Our experimental results indicate that maximum AM-PM distortion should be limited to 4-5° typically to ensure an average EVM of ~4-5% for the power amplifier, thus establishing a qualitative measure of phase distortion that is acceptable for linear PA operation. At the same time, excessive gain expansion (above 1dB), which often is accompanied by the dynamic phase distortion can also result in high EVM numbers and hence increased data packet error rate in the radio. It is therefore imperative to satisfy low AM-PM distortion in the design, along with moderate gain expansion, to achieve a balance between low EVM and high power-added efficiency (PAE) at low quiescent bias current.

III. Measured Results and Discussion

The results in this section are presented for a single design/fabrication iteration. The amplifier was designed with maximum on-chip/off-chip tunability in mind to allow performance optimization on an engineering test station. The critical interstage wire inductance was implemented as a bond-wire originating on chip and grounded on the paddle. Statistical analysis using Monte-Carlo simulations in ADS showed that given production variation, there may be a substantial variation in device characteristics. However, once the optimum wire parameters are established through the performance optimization, this shunt inductor can then be made on-chip to mitigate the risk of low production yield. The output series inductor is implemented as two separate wires bonded off-chip and back on to the chip. These wires cause much less statistical variation and are preserved to benefit from their high-Q.

A. Single-Tone and OFDM Characterization

Single tone performance was first assessed to verify the basic design of the PA. Figure 2 shows measured gain, harmonics and PAE versus single tone output power, demonstrating that original design targets were successfully achieved across the band at V_{M1}=2.7V, V_{M2}=2.85V, V_{CC}=3.3V. Next, linear performance was evaluated through AM-AM, AM-PM single-tone and EVM measurements using an OFDM modulated signal. Figure 3 shows measured EVM, AM-AM and AM-PM characteristics for one of our lower power designs that has been used for linear performance benchmarking. As can be seen, very low phase distortion results in a low riding EVM curve that, in this case, is primarily governed by the AM-AM distortion. One can also notice that the 2% EVM level occurring around the maximum gain point is due to the 0.5 dB gain expansion that happens just before the PA goes into compression. It is important to note that the total EVM shown is not an additive function of the residual system EVM and that contributed by the PA. The system EVM and the PA EVM are not statistically correlated, and hence, are not additive.

The EVM measurements in this work have been performed using Agilent Vector Spectrum Analyzer system. RF waveform is transmitted during T_{ON}=176µs internally triggered pulse with T_{OFF}=100µs idle time (no RF). Unless otherwise noted, the amplifier stays constantly biased. Average transmitted packet power is measured by a power meter with a properly set duty cycle. These waveform settings are used as a default by the Agilent Signal Studio. Average packet current is measured in reference to the 176µs transmit time to account for the quiescent current during the PA T_{OFF} time as follows: $I_{AVER}=(I_{MEAS}\cdot T_{ON} - I_Q\cdot T_{OFF})/(T_{ON}+T_{OFF})$, where I_{MEAS} is the total current consumption and I_Q is the amplifier quiescent current.

Measured EVM, PAE and average power gain for the PA are plotted in Figure 4 versus average modulated output power as a function of bias of the power stage. Two sets of bias condition are presented for the power stage to demonstrate the trade-off between the back-off EVM and maximum linear PAE. The driver stage is biased at 18mA in both cases. For the lower power stage bias (58mA), at P_{OUT} of 23.6dBm and EVM=4.4%, the amplifier delivers 22% linear PAE. For the higher power stage bias (88mA) the PAE drops by ~1% at a power gain premium of 0.7dB. Whilst giving up some PAE, the higher bias condition results in rather lower back-off EVM, e.g. at P_{OUT} of 18dBm the EVM is 0.8% lower than measured at the lower bias condition. Several of our customers have indicated that their radios typically achieve adequate data packet error rate at the EVM level of -27dB (4.4%), which is why this number is used here as a maximum specification level.

B. Correspondence of AM-AM, AM-PM to EVM

Fig. 5 shows corresponding measured AM-AM and AM-PM characteristics for the two bias conditions. For the lower bias at the peak gain point, the gain expansion reaches ~1.0dB and the phase distortion is –4.35°. These correspond to ~4.4% EVM per Fig. 4a reached right at the modulated gain peak – before the amplifier slides into the gain compression. For the higher bias, the modulated gain expansion is 0.5dB at the gain peak with a corresponding phase distortion of –2.6° that still correspond to ~4.4% EVM per Fig. 4a. However, due to the high peak-to-average ratio of an OFDM signal (9-12dB at 54Mbps data rate), the probability of the output voltage of the amplifier to dynamically swing into the compression region grows quite quickly as the output power approaches values of several dB below the compression. According to Fig. 4, dynamic compression of some of the high-power tones present within the input multi-tone OFDM signal begins to affect the EVM at P_{OUT} ~22.5dBm, which is 8dB below the P_{SAT}. Moving away from this point, e.g. at 20dBm, one can clearly see that 1° lower AM-PM and 0.4dB lower AM-AM characteristics yield a 0.8% lower EVM at the higher bias condition. Hence, one can conclude that overall lower dynamic AM-AM and AM-PM characteristics produce lower EVM curve. Specifically, to keep EVM below 2-3% the AM-AM and AM-PM distortions must be contained below 0.5dB and 2-3°, respectively.

C. Effects of Pulsing the PA

Thus far discussed results are representative of the continuously biased amplifier, where average DC current exhibits a transient from I_Q to I_{AVER} due to the framed nature of the input RF signal. In a WLAN transceiver, the PA is normally shut off during the receive cycle, principally to reduce system power consumption. Under pulsed bias conditions, thermal transients in HBT circuits may significantly degrade system performance as the current transitions from shutdown (10nA) to I_{AVER}. It is typically required that a PA performs well when pulsed without invoking amplitude tracking in the receiver.

The training sequence in the radio's receiver determines the signal amplitude during the first 10-20μs. It then locks in the receiver LO level and any variations in gain with time are interpreted as magnitude errors in symbols. Even such small power gain transients as ~0.3dB with time constants above several microseconds can cause time-varying symbol amplitude within received data packet, significant enough to degrade EVM to above 3-4%. It is therefore imperative to ensure fast PA switching with minimal gain transients, below 0.2dB. Such gain transients in the output PA signal can also result from poor current sourcing to the PA from a DC power source. Very good low-frequency terminations are required to establish fast current sourcing and minimize the base-band noise. As illustrated in Figure 6, this novel MMIC design performs equally well when operated under pulsed bias conditions. Only a minor degradation in EVM can be observed at all power levels. Temperature-compensated bias circuits, optimum HBT sizing (driver stage – 900μm^2, power stage – 4800μm^2) and optimized chip layout (with optimal location and adequate number of via holes on chip) help reduce thermal transients.

D. Comparison to Other Power Amplifiers

With the MMIC built in a 3x3mm QFN package with total height of 0.9mm, the part has good heat dissipation and only 7 low-cost external components. In comparison, a Skyworks Inc. 2.4GHz WLAN amplifier described in [3] is manufactured in a Multi-Chip Surface Mount Technology in a 4x4mm package with a total thickness of 1.5mm which also results in a higher cost. The bill of materials consists of 21 external components that take up significant area on-board. The PA in [3] produces a linear power of 23.7dBm at 4.4% EVM. Integrated power detector is present. Another interesting product was reported by Anadigics Inc. in [4]. Similar to [3], the amplifier in [4] is built on a laminate 4x4mm substrate with a total module height of 1.41mm. However, in contrast to [3], this PA only requires 2 external components. Linear performance demonstrated is 23dBm output power at 4.4% EVM and PAE of 20-22%. No integrated power detector is available. One of the advantages of this PA is the 3 stage design that allows achieve 30dB gain.

IV. Conclusion

In this article we presented novel linear power amplifier suitable for wider range 802.11b/g wireless applications. Specifically, the amplifier demonstrated good linearity of 4.4% EVM at a corresponding OFDM modulated output power with 54Mbps data rate of 23.6dBm and a high power-added efficiency of 22%. The MMIC is implemented in a cost-effective 3x3mm QFN leadless package that allows for a superior heat dissipation and requires minimal non-critical external components. The amplifier includes an integrated power detector and a shut-down circuit on-chip. Linear characteristics of the amplifier are achieved by rigorous modeling/design and reduction in AM-AM and AM-PM distortions. In addition, the amplifier shows excellent pulsed performance with minimal degradation in dynamic EVM.

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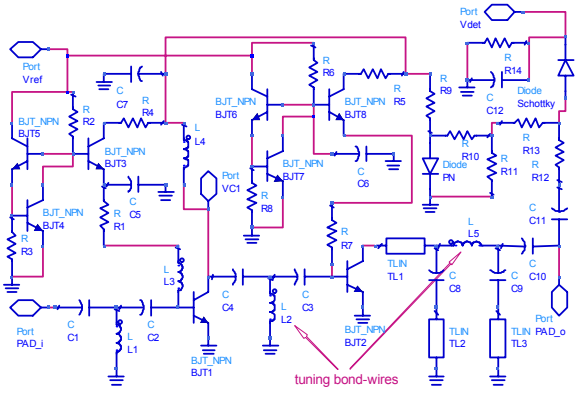

Fig. 1 Schematic of the MMIC. Shutdown circuit is not shown.

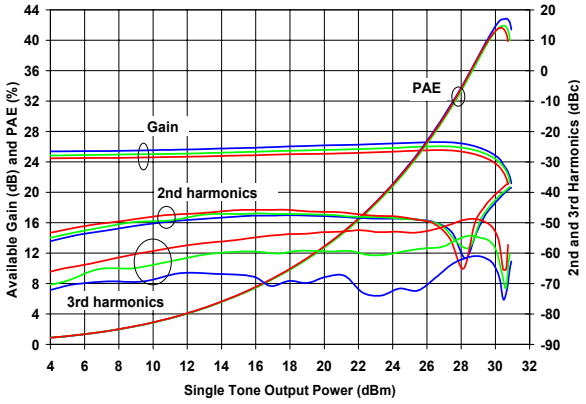

Fig. 2 Single-tone performance of the MMIC at 3.3V. Blue, green and Red represent 2.4, 2.45 and 2.5GHz curves. I_Q=78.5mA.

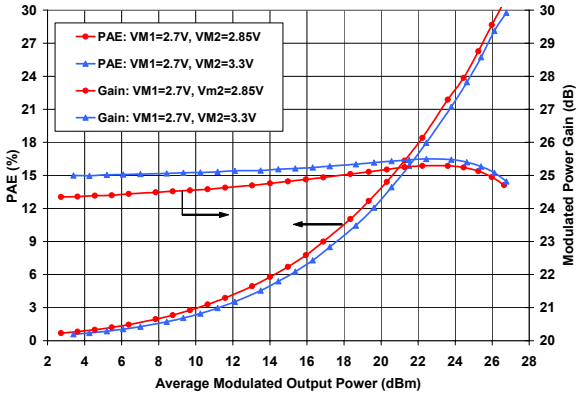

Fig. 4b Measured linear PAE and modulated power gain of the new MMIC at V_{CC}=3.3V. (●) and (▲) are for the low and high bias conditions, respectively.

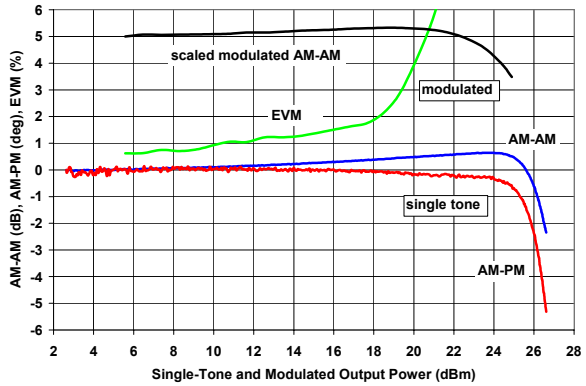

Fig. 3 EVM and AM-AM, AM-PM characteristics at V_{CC}=3.3V of the benchmark device. SS gain is 27dB at 2.45 GHz. The Modulated AM-AM curve is obtained by subtracting 22dB from the SS gain for graphing utility.

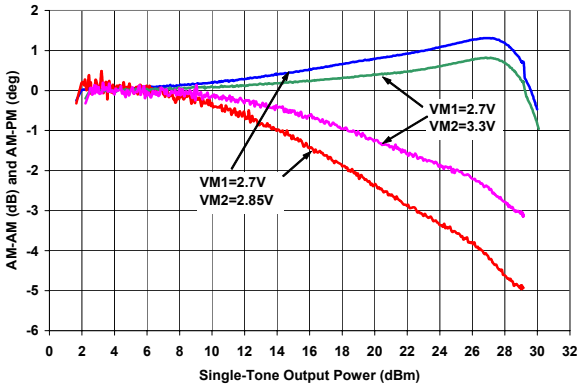

Fig. 5 AM-AM and AM-PM characteristics of the new MMIC measured V_{CC}=3.3V and 2.45 GHz. Two bias conditions are presented for the power stage (see in the text).

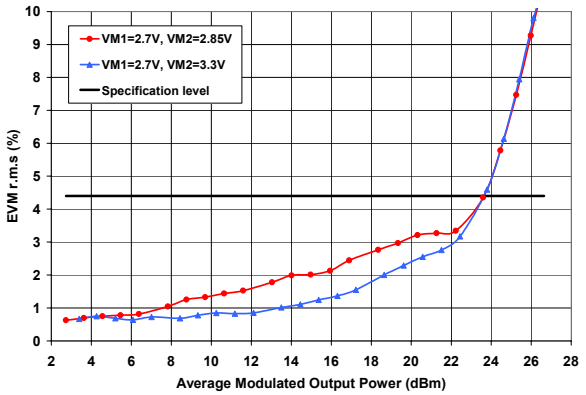

Fig. 4a Measured EVM of the new MMIC at V_{CC}=3.3V. (●) and (▲) are for the low and high bias conditions, respectively.

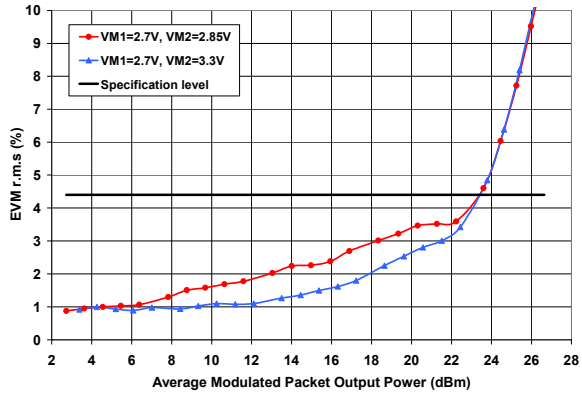

Fig. 6 Measured EVM under pulsed bias condition. VCC=3.3V, f=2.45GHz. VM1,2 are pulsed from 0V to their respective values. Input RF signal is delayed by 1µs from the positive edge of DC pulse.