The Integrated 2W High Voltage/High Power 0.12-µm RF CMOS Power Amplifier

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***ABSTRACT* — A 2W HiVP power amplifier for GSM mobile communication system is designed using 0.12-µm CMOS process. To solve the problem of low breakdown voltage in deep-submicron CMOS technology, the new High Voltage/High Power (HiVP) device configuration is used. With HiVP configuration, a large voltage can be divided by several devices, so that the voltage drop on each device is reduced. Hence the low-cost CMOS technology can be adopted for the design of power amplifier which will be used in a mobile phone. In this paper, an analytical overview of theory and practice of the HiVP power amplifier are discussed.**

I. INTRODUCTION

Due to the substrate parasitic capacitance and resistance, Gallium Arsenide (GaAs) has been used to implement most RF power amplifier that operate in the Gigahertz band. On the other hand, standard digital technology has seen a breakthrough in both performance and size through the use of device scaling to deep-submicron CMOS. For certain highly-integrated, low-power, wireless transceivers operating at several GHz, CMOS is also attractive to implement RF circuits. The power amplifier is an indispensable component in the wireless communication system, which is simultaneously a design bottleneck in the deep-submicron CMOS process. The output power of the mobile phone in GSM system should be about 2 W [1]. On the other hand, the typical maximum allowable voltage of a 0.12-µm CMOS transistor is only close to 1.5 V. The gate-drain voltage of a MOS transistor is especially critical due to the field distribution along the channel and the extreme thin gate oxide. This restriction limits the power at the output of a single conventional transistor. The HiVP [2] is a High Voltage and High Power device configuration in which several devices are connected DC and RF in series, so that the large output voltage can be divided by all the cascaded devices. With some improvements, which will be shown later, it is even possible to share the large voltage equally.

Because the transistors are all connected in series, the same current flows through all of them in a row. Simply due to the increasing impedance from bottom device to top device, which is seen by the drains of each individual device, the drain voltages of each device are different. Therefore the HiVP configuration is also a very ideal power combiner. The output power of this configuration is the combined sum of all powers achieved from each individual device, therefore, a high output power is achievable.

Section II discusses the functional principle of the HiVP configuration in detail. Section III presents the CMOS power amplifier design using the HiVP configuration and the simulation results.

II. HIVP CONFIGURATION

Figure 1 illustrates the construct of a CMOS HiVP configuration. Several devices are connected DC and RF in series. Therefore the currents flowing through the transistors are all the same. Ideally the transistors have the same operating points. The resistors R_2-R_5 are used as voltage divider to ensure that the DC voltages between the drain and the source V_{ds} of each device are exactly the same. The DC voltage V_{ds} of T1-T3 are equal the DC voltage drop of R_2-R_4, however, the DC voltage V_{ds} of T4 is equal the DC voltage drop of R_5 plus the gate-source voltage of T4. Therefore, R_2, R_3 and R_4 should have the same value where R_5 should be much smaller than the others. The DC voltages between gate and source of all the devices are always the same and equal to V_{gg}, because the devices are identical and the same current flows through them. The resistor R_5 serves simultaneously as a feedback to allow the gate voltages of each device to swing with the RF output signal. Hence the voltages between gate and drain of each device can remain smaller than the maximum allowable voltage between the terminals of the transistors.

The two inductors L_g and L_d serve as RF choke which feed DC power to the gate and drain. L_d must be large enough so that the current through it is substantially constant.

The capacitors between the gates of the floating MOS transistors and the ground C_2 - C_4 adjust the impedance level seen by the drains of each individual device, which is equal to the impedance at the source input of the upper device. The calculation of this impedance can be done by using a current source at the source of the device as shown in Figure 2 a). The small-signal equivalent circuit is shown in Figure 2 b). C_{shunt} symbolizes C_2 - C_4 in Fig. 1. Z_{source} indicates the impedance seen by drains.

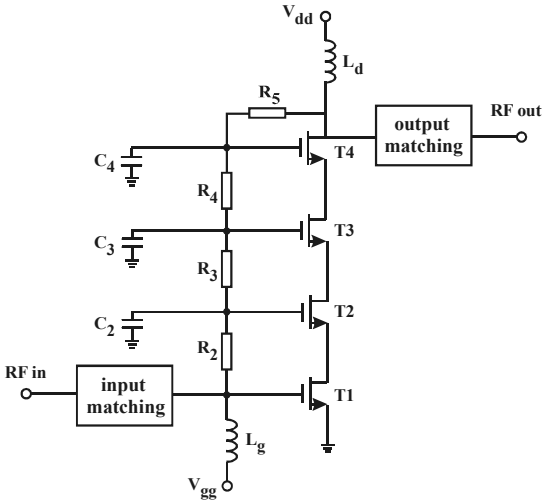
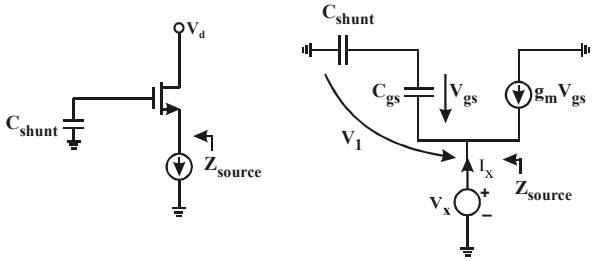


Figure 1: A HiVP configuration with four devices.



C_{shunt}: The shunt capacitance between gate and ground

Figure 2: Calculation of the impedance seen by the drain.

Noting that

$$V_1 = -V_X, \tag{1}$$

we have

$$V_{gs} = \frac{1/j\omega C_{gs}}{1/j\omega C_{gs} + 1/j\omega C_{shunt}} * V_1$$

$$= -\frac{C_{shunt}}{C_{shunt} + C_{gs}} * V_X . \tag{2}$$

Following

$$I_X = -V_{gs} * (g_m + j\omega C_{gs}) . \tag{3}$$

Substituting Equation (2) into Equation (3) yields

$$I_X = \frac{C_{shunt}}{C_{shunt} + C_{gs}} * (g_m + j\omega C_{gs}) * V_X . \tag{4}$$

This leads to the impedance at the source input of the device

$$Z_{source} = \frac{V_X}{I_X} = \frac{1}{g_m + j\omega C_{gs}} * \frac{C_{shunt} + C_{gs}}{C_{shunt}} . \tag{5}$$

If the transistor has a gate width of several millimetres, the gate-source capacitance has normally a value in the range of several pF. Therefore $j\omega C_{gs}$ at several gigahertz is much smaller than g_m (typically 1-5). Z_{source} can be approximately given by

$$Z_{source} \approx \frac{1}{g_m} * \frac{C_{shunt} + C_{gs}}{C_{shunt}} = \frac{1}{g_m} * (1 + \frac{C_{gs}}{C_{shunt}}) . \tag{6}$$

Observe from equation (6) that C_{shunt} is the unique but useful variable to adjust the impedance level seen by the drains of each individual device. The smaller C_{shunt}, the larger is Z_{source}. For a high output power, the voltage swing of the top device must be large enough (e.g. peak-peak voltage > 10 V shown later) . On the other side, the voltage swing of the bottom device must remain small (peak value smaller than 1.5 V) because the source of the bottom device is directly connected to ground. For an equal distribution of the large drain voltage of the top device, the higher devices must have larger voltage swing. Because all the devices are connected in series, the same current flows through them. A larger voltage swing can only be obtained with a higher impedance level seen by the drain. Therefore, according to equation (6), gate of a higher device must be connected with a smaller capacitor, which means that the condition

$$C4 < C3 < C2 \tag{7}$$

must be fulfilled.

III. HiVP Power Amplifier Design

For mobile phones, a linear power amplifier using 0.12-µm CMOS technology is designed. The required output power is 2 W on 50 Ohm load at 1 GHz, with a 3.6-V DC power supply.

Due to the high output power, the 3.6-V DC power supply should be fully utilised. On the other hand, the maximum allowable voltage between the terminals of a transistor is only 1.5 V. To reduce the voltage drop on a single transistor, HiVP configuration can be adopted. If the operating point is selected at V_{ds} = 0.6-0.9 V, 4-6 transistors can be connected in series which can share the 3.6-V DC voltage together. The DC-simulation result, which is shown in Fig. 3, indicates that HiVP can be considered as a single transistor. The gate of the first cell can be considered as the input and the drain of the top cell as the output. The difference between such a configuration and a single conventional device is the ability to carry a much larger DC voltage.

Due to the low DC supply voltage, an impedance transformation at the output, namely from 50 Ohm load to a smaller resistance R shown in Fig. 4, is required. The maximum value of R is

$$R_{\max} = \frac{V_{dd}^2}{2P_{\max}} = \frac{(3.6)^2 V^2}{2 \cdot 2W} = 3.24\Omega \tag{8}$$

Such an impedance transformation is quite difficult to implement due to the small value of R. Therefore, the input and output matching networks are designed to be off chip to increase the matching flexibility and avoid excessive power loss of on-chip inductors.

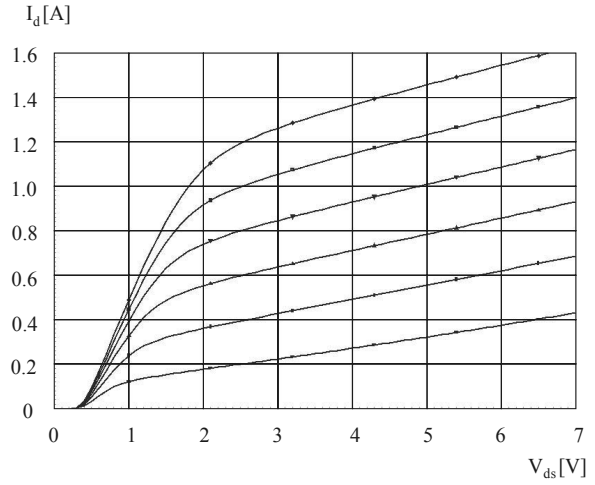


Figure 3: DC simulation results for the HiVP structure with four devices.

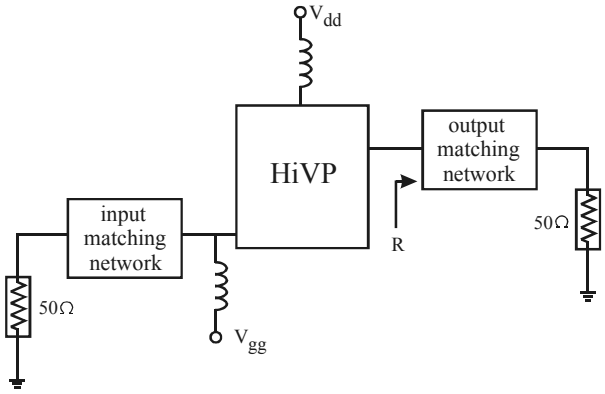


Figure 4: Impedance transformation at output.

With the 3.24 Ohm load, the peak RF current will not exceed $V_{dd}/R_{max} \approx 1$ A, and the DC drain current bias must be set approximately to this value. Since the peak drain current is the sum of the bias and peak RF current, the transistor must be designed to supply about 2 A with minimum voltage drop. A total device width of several millimetres would therefore be required. A compact layout for so large devices, such as waffle MOSFET is already discussed in [3].

As a compromise for linearity and efficiency, a class AB power amplifier was designed. The DC operating point should be optimized, so that the distortion of the output signal can be minimized.

If we have many devices in series and the DC supply voltage is not sufficiently high, it is quite difficult to adjust the operating points to ensure that the drain to source voltages are all the same. This is above all an essential problem by the top device. The minimum value of V_{ds} of the top device is equal the gate-source voltage of itself when $R_5 = 0$ Ohm. If V_{gg} is e.g. fixed at 1 V, the minimum value of V_{ds} of the top device is 1 V. If four devices are used in our HiVP, we have then at most 3.6 V – 1 V = 2.6 V to share in the lower three devices. Each device can obtain at most 0.87 V as V_{ds}. But this problem is not very critical. If it is ensured that all the devices work in the saturation range, the current flowing through them is nearly the same.

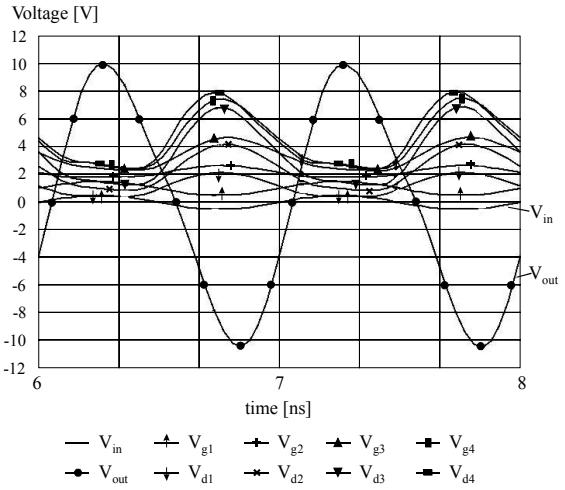


Figure 5: Voltage waveforms versus time.

The RF signal is applied to the gate of the first device. Due to the inductor L_d at the drain of the top cell, the DC voltage at the drain of the top device is equal to the supply voltage with an RF voltage swing around this value. At maximum output power, the voltage at this drain swings down close to zero and up to twice V_{dd} or even more, if the matching network at the output has a tank circuit [4]. The main problem is to divide this large drain voltage equally to all the devices. As an example of an unequal allocation are the voltage waveforms in time domain of a HiVP power amplifier with four devices illustrated in Figure 5. The resistors of the voltage divider are defined, so that all the four devices have the same operating points. In this case, R_5 must be much smaller than all the other three resistors.

Obviously, 10 V output voltage, i.e. 1 W output power on 50 Ohm is achieved. The RF voltage swing at the drain of the top device T4 has a peak value of about 8 V. This voltage should be equally divided by all the devices. But this condition and the condition that all the V_{gd} are smaller than 1.5 V are not satisfied. The first problem arises from T1. The gate voltage and the drain voltage are out of phase. This involves a magnitude of V_{gd1} of about 1.65 V. The problem occurs also at T3. The maximum magnitude of the RF voltage V_{gd3} is about 2.2 V, though the gate voltage and the drain voltage are in phase.

To overcome these problems, the resistances of the voltage divider should be changed, so that the DC operating voltages are optimized. Due to the very small value of R_5, the difference between V_{d4} and V_{g4} is very small, which involves that the drain of T3 has a very high DC operating point, hence the magnitude of V_{gd3} is very large. If we e.g. increase R_5, the DC operating voltage of drain of T3 can be reduced. The DC operating voltage of gate of T3 is also reduced, but only with a smaller amount. Therefore the difference between V_{d3} and V_{g3} is reduced. Figure 6 illustrates the simulation result, which indicates that the maximum magnitude of V_{gd3} is reduced to 1.6 V. Simultaneously the maximum magnitude of V_{gd1} is also reduced to 1.4 V. Further improvements can be obtained, if the other resistances are also varied. In this case, the DC operating points of the devices are no longer

identical. But the performance of the power amplifier will not be significantly degraded, if it is ensured, that all the devices operate in the saturation range. It is here important to see that an equal division of the large drain voltage of T4 is possible.

The method mentioned above provides a method for equal voltage allocation. If 2 W output power on a 50 Ohm load is desired, 14 V output voltage should be achieved. This means, even larger RF voltage at the drain of the top device should be divided. In this case, more devices should be employed in series. But if too many devices for voltage division are used, the DC supply voltage is not high enough to assure that all the transistors operate in saturation range.

For the desired 2 W output power six devices are used. The final simulation result of voltage waveforms in time domain is illustrated in Figure 7. It can be seen that 14 V output voltage is achieved with a input voltage of 0.6 V. The large voltage at the drain of the top device can be equally divided by all the devices. V_{gd} of all the devices remain smaller than 1.5 V.

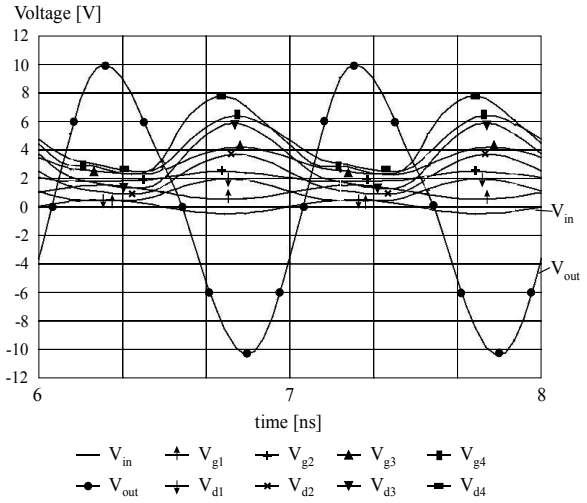


Figure 6: Optimized voltage waveforms versus time

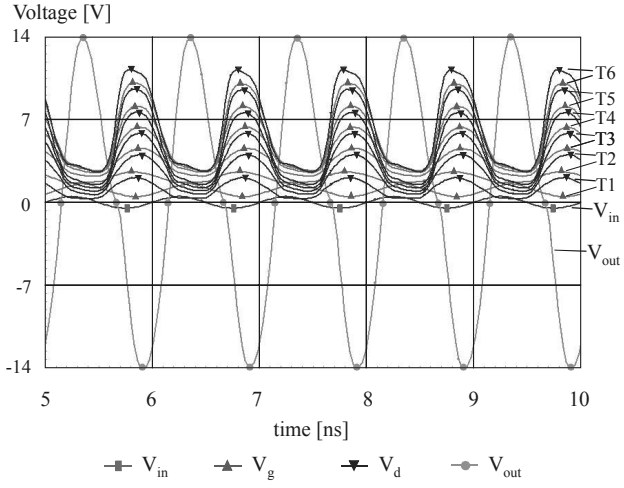


Figure 7: Voltage waveforms versus time for 2 W output power on 50 Ohm at 1 GHz.

According to the DC simulation results, the DC-current is about 1 A. Thus the power added efficiency PAE can be calculated by

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \approx \frac{2W - 0.0036W}{3.6V \cdot 1A} \approx 55\% \cdot \qquad (9)$$

The input-referred output power is presented in Fig. 8. The output referred 1-dB compression point is approximately 34 dBm.

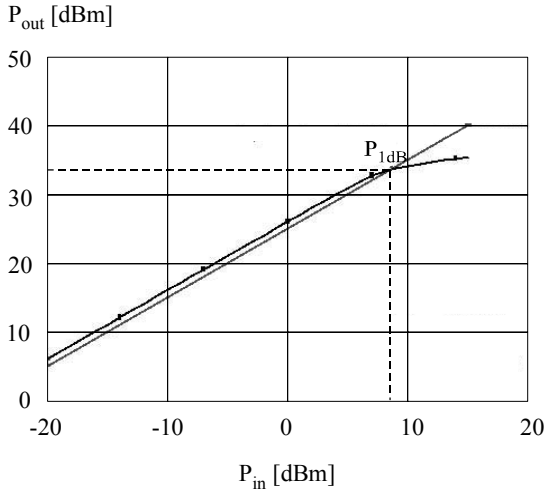


Figure 8: Power transfer curve at 1 GHz.

IV. Conclusion

The advantage of the HiVP configuration used here is the equal division of a large voltage, which solves the problem of low breakdown voltage in deep-submicron CMOS technology. Therefore, with HiVP configuration, deep-submicron CMOS technology can prove to be a feasible process to implement power amplifiers used in mobile phones, which offers a possibility for a monolithic integration in CMOS transceiver system.

Naturally, HiVP configuration can also be used in another ranges, e.g. satellite communication. If the DC supply voltage is sufficiently high, an increase of the optimum output matching impedance close to 50 Ohm is possible, which is optimal for all planar transmission lines and enables one to design a broadband power amplifier.

References

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